Wafer scale technology to integrate photonics on BiCMOS electronics

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In this publication we describe our technology to integrate a standard indium phosphide (InP) photonic membrane, with a thickness of several micrometer, on a fully functioning electronic BiCMOS wafer. This technology is demonstrated here for the first time.

Introduction

The integration of a photonic circuit on top of an electronic circuit reduces the physical distance and enables a new design dimension for electrical connections. Short interconnects are a key requirement to increase the electrical bandwidth and reduce electrical power consumption. A good performance in the electrical domain corresponds, in case of a transceiver module, to a higher communication bandwidth. Within the European "WIPE" project [1] we developed a technology to increase the bandwidth of a transceiver by integrating photonics with electronics on a wafer level. Here we describe the process steps used for demonstrating this wafer level technique for the first time.

Wafer material description

The demonstrated integration process is performed completely on wafer level within a III - V cleanroom. The technology uses an adhesive wafer bonding approach based on [2]. The starting point is the two wafers from the two different domains: photonics and electronics. The photonic wafer is based on InP and has a wafer diameter of 3 inch. The electronic wafer is fabricated in a 0.25 μm SiGe:C BiCMOS process on a 200 mm wafer (8 inch). Both wafers are based on mature foundry processes. At the end of the process the InP membrane, containing the photonic ICs, is bonded to the BiCMOS wafer, containing the electrical circuits. Both layers are electrically connected by interconnects through the InP membrane.

For the integration a few adaptions have to be made to enable wafer to wafer alignment and post processing. As the InP substrate will be removed wet chemically after the bonding process, an additional etch stop layer has to be included below the InP foundry's standard epitaxial layer stack. Additionally several features and structures have to be etched through the standard layer stack during the foundry process, which will be used for the final chip separation and as marker structures during the process.

The only modification needed on the BiCMOS wafer is a matching wafer size. As the process is performed with tools designed for 3 inch wafer handling, from the 8 inch BiCMOS wafer 3 identical 3 inch wafers are cut. The designs on both wafers match each other, which is obtained by designing the InP wafer based on the layout of the BiCMOS wafer.

Integration process

Preparation wafer alignment

The alignment of both wafers relative to each other is a key requirement to create functioning hybrid devices. In [3] a comparison of different alignment techniques is

presented. The one used for this demonstration is the backside alignment (BSA) technique. Thereby features of the backside of one wafer are aligned to matching structures on the topside of the other wafer. None of the wafers originally includes structures on the backside. These need first to be realized on the backside of the InP wafer. This wafer preparation process starts with protecting the topside of the InP wafer with a thick layer of photoresist (PR) which is applied by spin coating. Next the backside of the wafer can be processed. The markers for the wafer-to-wafer alignment are etched into the InP wafer. For this the backside is first cleaned with an oxygen based plasma. Next a silicon dioxide (SiO_2) layer is deposited with an ICP PECVD process. This dielectric layer will be used as a hard mask and is pattered by using a photoresist and contact lithography. For this a chromium mask is aligned to the topside of the InP wafer, which includes the wafer-to-wafer alignment features. The pattern of the PR is transferred into the SiO_2 with a dry etching step. Subsequently the pattern of the dielectric layer is etched into the backside of the InP wafer using a plasma etch, based on a gas mixture of CH_4 and H_2. To complete the InP wafer preparation the SiO_2 layer from the backside and the PR protection layer from the topside are removed.

Wafer-to-wafer bonding

The wafer bonding uses benzocyclobutene (BCB) as adhesive bonding material. To increase the adhesion of BCB a thin SiO_2 layer is deposited on both wafers. To prevent gaseous products to interfere during the bonding process an outgassing step of 1 hour at 240°C in a N_2 atmosphere is performed. Afterwards the adhesion promoter AP3000 is applied by spin coating, followed by spinning BCB with thicknesses of 8 µm on the BiCMOS wafer and 16 µm on the InP wafer. These thicknesses are at least double the topologies on the two wafers (see [2]). The BCB layer on the BiCMOS wafer is additionally pre-cured to a value of 40 % crosslinking by placing it in a N_2 atmosphere for 1 hour at a temperature of 175 °C [2]. The wafers are then aligned to each other and bonded under vacuum with a bonding force of 700 N. After releasing the force the chamber is filled with nitrogen up to a pressure of 800 mbar and heated to 240 °C. The bonded stack remains in the chamber under these conditions for 10 hours to fully crosslink the BCB adhesion layer.

Substrate removal

After the successful bond the combined stack is processed further to create the actual hybrid modules. Therefore the InP substrate has to be removed. To do so it is important to remove existing BCB pollution first by using a dry etch cleaning step. Next the InP substrate can be resolved in a solution of HCL and H_2O in the ratio of 4:1. This process is self-limiting and ends on the etch stop layer. Subsequently this sacrificial layer is removed wet chemically using a solution of H_2SO_4:H_2O_2:H_2O in the ratio 1:1:10. The actual membrane remains and the deep etched structures, like the markers and dicing lines, become visible. These features are filled with BCB and are therefore protected during the wet chemical etch stop layer removal.

Creation of interconnects and heat sinks

The next task is creating electrical interconnects between the two wafers. First windows are etched through the InP membrane to expose the underlying via pads. A dry etch is used to achieve this. Therefore a SiO_2 layer is deposited on top of the InP membrane which will be used as a hard mask. Subsequently PR is spin coated and patterned by

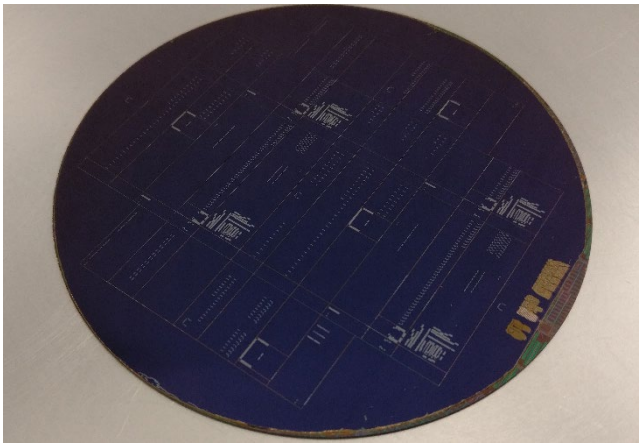

Fig. 1: Photronic wafer (BiCMOS wafer with InP membrane) with SiO_2 hard mask (dark blue) for etching windows into the InP membrane

contact lithography. After transferring the pattern into the hard mask using a dry etching step, the remaining PR is removed and the InP membrane can be etched. In figure 1 the bonded stack is shown just before etching the windows into the InP membrane.

After the etching the InP contacts are immediately accessible, while the BiCMOS contact pads are still covered with BCB. The BiCMOS pads have to be opened to allow the electrical interconnects. The BCB layer has a thickness of 24 µm. The electrical interconnects will be created by electro-plating which requires smooth transitions from one level to the other [4]. The two pads to be connected are therefore displaced with respect to each other. The edges of the pads are separated by at least 20 µm. This distance is reserved for a sloped sidewall which is smooth enough to enable electro-plating. The sloped sidewall is created during the BCB etch. For this a 24 µm thick layer of positive photoresist is used. This PR reflows during the dry etch due to the increased chamber temperature. This creates a slope in the PR which is transferred into the BCB. To etch through 24 µm thick BCB a single layer of 24 µm PR is not sufficient. Testing several approaches lead to the conclusion that the best result is achieved by etching first 50 % of the BCB layer, followed by cleaning the wafer and repeating the complete step, starting with spinning of PR, executing the lithography again and etching through the remaining BCB. This can give a small step in the slope, which has no influence on the following processing.

The last step is the electroplating. The wafer surface is first cleaned, after which a seed layer is deposited with e-beam evaporation. The seed layer consists of 50 nm titanium and 100 to 200 nm gold. This layer is covering the whole wafer. A photoresist layer is spin coated to define the areas for electro plating, using contact lithography. After electro plating 2.5 µm of gold, the remaining PR is removed. The gold part of the seed layer is then wet chemical removed by potassium cyanide (KCN). Subsequently the titanium is removed by using oxalic acid.

Figure 2 shows a photograph of the created assembly, presenting the etched structures used to access the photonic (gold) and the electronic (aluminum) contact pads. Additionally several plated structures are visible, like a heat spreader on the top right hand side of the picture. The InP is divided into single islands by the predefined dicing lines. By sawing the BiCMOS along these lines the separate hybrid modules are obtained. The lines have a width of 50 µm and the sawing blade removes 40 µm.

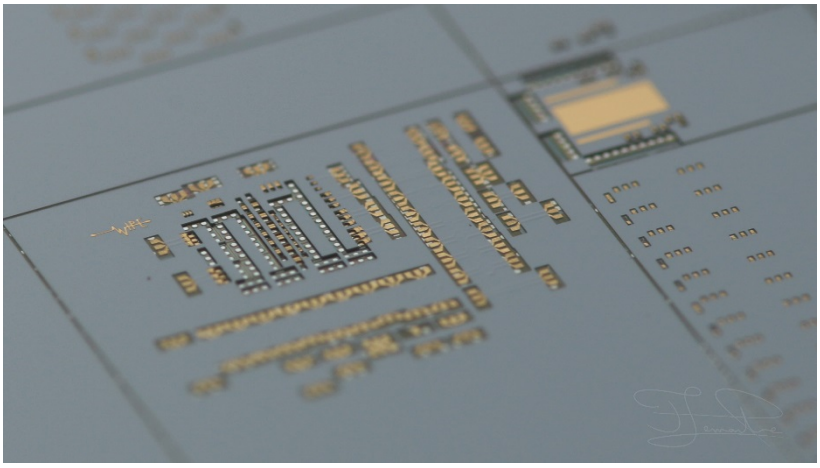

Figure 2: Picture of the InP based photonic membrane layer with windows to access and interconnect the photonic (gold) and the electronic contact pads (aluminum). Photo by Florian Lemaitre

Conclusion

In this publication we presented the technology used to integration a standard InP photonic membrane, with a thickness of several micrometer, on a fully functioning electronic BiCMOS wafer. The requirements regarding the wafer material are defined and the process is described with the main steps: preparation wafer alignment, wafer- to- wafer bonding, substrate removal, creation of interconnect and heatsinks and a brief description on the separation of the single devices. The created devices are undergoing characterizations and show promising performance.

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References

[1] European commission, http://cordis.europa.eu/project/rcn/199492_en.html; 16/09/2019
[2] M. Spiegelberg, J.P. van Engelen, T. de Vries, K.A. Williams, J.J.G.M. van der Tol, "BCB bonding of high topology 3 inch InP and BiCMOS wafers for integrated optical transceivers" in Proceedings of the 23nd Annual Symposium of the IEEE Photonics Society Benelux Chapter, pp. 160-164, 2018
[3] F. Niklaus, G. Stemme, J.Q. Lu, R.J. Gutmann, „Adhesive wafer bonding", Journal of Applied Physics, vol. 99 - 6, pp. 031101/ 1 -28, 2006
[4] A. Meighan, M.J. Wale and K.A. Williams, "Low resistance metal interconnection for direct wafer bonding of electronic to photonic ICs," in Proceedings of the 22nd Annual Symposium of the IEEE Photonics Society Benelux Chapter, pp. 116-119, 2017.