Butt joint in top layer for low loss waveguides

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We present a new integration scheme for the InP based platform to monolithically integrated low-loss passive waveguides in the SMART photonics integrated circuits (PICs) platform. This method consists of performing a butt joint in the top layer of our wafers. This allows to have two different top claddings on the same wafer, one heavily doped optimized for active and one undoped optimized for passive elements. In PICs doping is necessary to allow electrical contacting of active components such as lasers, photodetectors and modulators. The dopant elements are known to cause intraband optical absorption with optical losses of more than 3dB/cm being common. Our simulations suggest losses as low as 0.6 dB/cm with the optimized top claddings. We have experimentally verified the differences in losses between the different layerstacks. We fabricated four wafers and measured the losses: one wafer has a standard layerstack, two wafers the new integration scheme and a reference wafer with no top cladding doping. We measured losses associated to three different widths of deep waveguides. We discuss the results and propose improvements.

Introduction

Low losses waveguides are necessary for a variety of applications such as sensing [1], delay lines [2] and many others. Usually, when extremely low optical loss values are necessary, silicon nitride (SiN) based platforms are the one performing better with losses as low as 0.03dB/cm [3]. However, they present a main drawback: active components such as lasers, amplifiers, detectors and electro-optical modulators are not available in such platforms, limiting their potential. InP based platform is an alternative, it is a direct bandgap semiconductor which allows the monolithic integration of active and passive components on the same chip. This eliminates the requirement for an external light source making the final product potentially lighter, smaller and cheaper. Compared to SiN however, losses are in the range of 2-4 dB/cm [4]. In this platform we can identify three major sources of optical loss: intrinsic losses, surface roughness and doping loss. Intrinsic loss[5] are connected to the refractive index of InP, not much can be done to control this contribution, but it is important to have a defect free material to avoid to make this losses even higher. With different lithography and etching techniques, waveguide wall roughness can be made smooth (or even removed with wet etch techniques) thus reducing roughness as source of loss. The third source is the presence of doped material. This mechanism is analyzed below and it is the main source of losses we focus on this paper.

Smart Platform

Starting from a InP substrate, different layers of InP, InGaAsP and InGaAs are grown. These layers have different optoelectronic properties and form the so called layerstack [4]. Trough different fabrication steps, optical elements such as laser, detectors, modulators and waveguides are pattered in the chip creating a PIC. We can identify three main layers: the substrate, the core and the top layer. The core layer is where the optical mode propagates and it is made of the quaternary alloy InGaAsP. The concentration ratio of the four elements controls the semiconductor bandgap and refractive index and allows for light generation and guiding at chip level. The top layer serves has a spacer between metal connections and the core layer that would otherwise suffer from high loss. A trade off in the layerstack is needed to make all the components available, mostly between active and passive devices. One of the most important is the dopant concentration in the cladding layers. In the next section we explain how this doping is necessary for good electrical

connections and excellent performances of active components, but also the trade off regarding losses on the passive waveguides.

Doping and its impact

Doping has an impact on several PIC elements and choosing the optimal doping profile for the layerstack involves many tradeoffs. When a p doped layer is grown on a n doped layer a *p-n* junction is created. *pn* junctions (*p-i-n* junctions to be more precise) are fundamental for havig semiconductor optical amplifiers (SOA) and phase shifter (PHs). SOA exploit the stimulated emission to amplify a light source, this is possible when electron-hole pairs are created in a semiconductor and recombines when stimulated by an incoming light source. A positively biased *p-n* junction allows to inject efficiently carriers and amplify light. Doping directly affects the number of carriers injected because it affects the resistance of the semiconductor. Resistivity of InP can be computed via the formulas[6]:

$$\rho_n = 10^{-0.918\log(n)+13.88}\ [\Omega cm]$$
$$\rho_p = 10^{-0.971\log(p)+16.19}\ [\Omega cm]$$

Where ρ_n is valid for negatively doped InP and ρ_p for positively doped. We observe that higher doping concentration results in lower resistance, this is beneficial for the performance of the SOA because it is leading to a low driving voltage and low power dissipation. PHSs benefit from doping as well: PHSs work thanks to electro-optical effects induced by a reversly biased p-i-n junction. Reverse biasing creates a charge depletion at the semiconductor interfaces that leads to the build up of an electric field [6]. This electric field together with charge depletion induces a refractive index change in the material. Such change can be exploited to change the phase of an optical mode propagating in the device creating a phase modulator. To have an efficient device the depletion region of the junction must overlay as much as possible with the optical mode to maximize the change in refractive index. A good overlap between the optical mode and the electric field is obtained when the p dope front is at the edge of the waveguide core. A key figure of merit for PHSs is V_π, defined as the voltage that creates a phase shift equal to π compared to the unbiased PHS. Having V_π low is crucial for a fast modulation of the PHS because it easier to be achieved by the RF driver. Same as in SOAs, doping reduces the semiconductor resistance, lowering as well the V_π. Doping however has a drawback: it increases the intrinsic losses of InP material. This loss are due to intervalence band absorption and has been well explained in literature [5]. So far in the SMART platform, there was no effective method to limit the doping only in the layerstack of active elements. Therefore, doped cladding is used along all the wafer increasing losses of passive elements as well. In the following section we describe how doping can be localized only where needed.

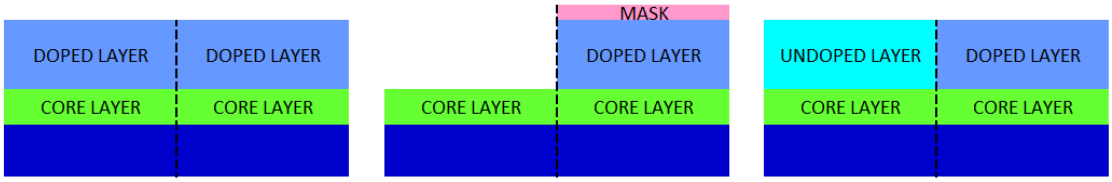

Figure 1 Visualization of the butt-joint process in top waveguide layers

Butt-joint technique and performance simulations.

Butt-joint allows to have different layerstacks on the same plane by growing and etching selectively portions of the wafer. In Figure 1 we show how it is done. Layers are epitaxially grown on wafer substrate up to a predetermined height. Then, a hard mask is deposited on wafer surface and trough a photolithography and etching process it is opened where we want to grow a different layer. The etch of the semiconductor is performed, and with the hard mask still in place, new layers are grown up to the height of previously deposited layers in the areas not opened in the hard mask. After removal of the hard mask, remaining shared layers can be grown on the entire wafer. Butt-joint is already implemented in the Smart platform to integrate the core active and passive core layers. However, for the first time, we performed a butt-joint in the cladding layers of the wafers to confine doping only in active region, thus strongly reducing loss. The impact on losses of this technique have been simulated with the commercial software Lumerical™: we use the Smart layerstack and we run different simulations with different thicknesses of the butt-joint on the top layers. In Figure 2, the blue line represents the results of the simulation. From the simulation we observe that a thickness of *1200nm* is required to reduce losses at their minimal. It is worth to mention that the losses by surface roughness can not be effectively simulated.

Experimental Methods

In our experiments we used 4 different wafers: two wafers have respectively a butt-joint height of 1200nm (*Wafer B*) and 800 nm (*Wafer C*). We have decided to test different thicknesses to determine the fabrication feasibility of this method. One wafer has a standard layerstack (*Wafer A*) as reference. We also have a benchmark wafer (*Wafer D*) with non intentional doping to determine the best achievable scenario. On the wafers we have deep waveguides with two different widths (*1um* and *1.5um*). With an external laser, light is coupled to the waveguides and we measure losses of single waveguides with the Fabri-Perot method [7]. In wafers with the butt-jointed methode, high doped island of different lengths are presents along the waveguides. This can let us extract the impact of doping directly as a function of the highland length[7].

Results

In Figure 2, on the left we report measure loss. Red circles represent the *1μm* wide waveguide while black asterisk are *1.5*μ*m* wide. The blue continuous line has been generated with simulations. The results are not the one expected since the simulated

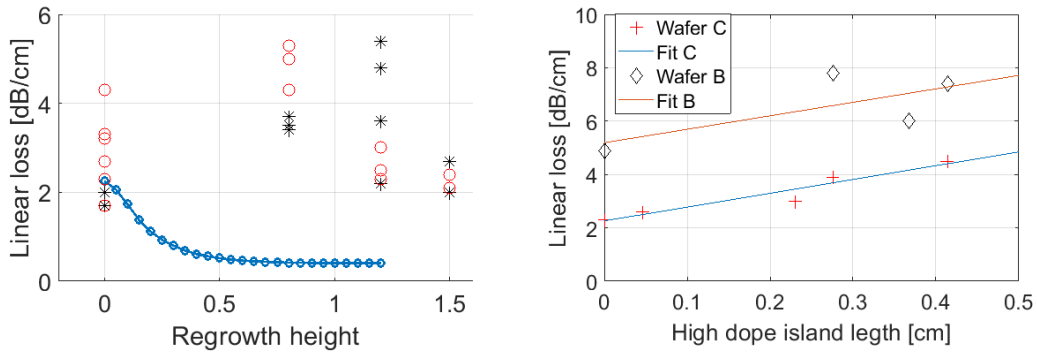

Figure 2: Left side: comparison of real data against simulation. Right: impact of doping on single wafer

behavior is not reproduced by data. Moreover wafer *Wafer A* (the one with the standard

layerstack) is the one with the lower losses. If we look at the right plot of Figure 2 at *wafer B* and *wafer C* where the but joint has been performed, we see that as expected waveguides with longer high dope region experience higher loss and that such contribution increases linearly when the length of the high doped island is increased. Both fitting lines have similar slope indicating that the losses of doping are similar. By inspecting the cross section of the fabricated waveguide we observed that the wafer A (standard process) has a nice sidewall roughness (Figure 3a), whichs is not the case of the

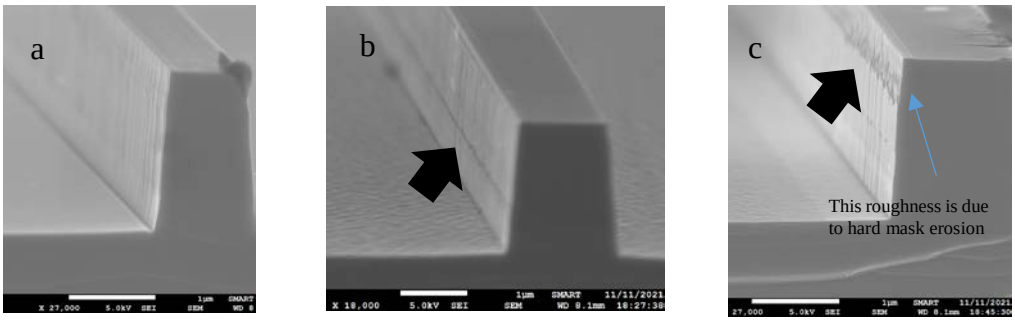

Figure 3 SEM Imaging of waveguide cross section for Wafer D , Wafer C and Wafer B

other wafers (Figure 3b-c) where an etched entrance is visible close to the core layers. This entrance is located on the interface of doped and non doped area. The transition between the doped area creates extra roughness that affect the optical losses. This feature needs to be solve to exploit the low intraband losses the non doped material can allow.

Conclusion

We have presented a new method of creating low loss waveguide on the Smart InP photonics integration platform. The method consisting on separating doped and non doped top claddings by a butt-joint regrowth on those layers. We fabricated few wafers and measured the losses. The losses are higher than expected, but they can be related to extra roughness creates by the interaction of the new process steps and the etching process. Further optimization on the integration scheme are necessary but once optimized this method will lead to lower loss waveguides.

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