Self-aligned flexible waveguides for interfacing flip-chip assembled InP photonic integrated circuits on SiN

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Scalable and cost-effectively connecting optical inputs and outputs to photonic integrated circuits (PICs) is challenging in photonic assembly. We utilize a TriPleX (SiN) interposer with suspended waveguides for interfacing optical fiber arrays to waveguides on InP PICs. Spot size converters on TriPleX are employed for high coupling efficiency. We apply this method in a multiport photonics assembly concept, in which an InP PIC is p-side-down soldered on the TriPleX carrier, which simultaneously provides electrical and optical interconnection. A design is made to deliver up to 112 optical interfaces between the TriPleX interposer and InP PIC. Designs and preliminary measurement results are presented.

Introduction

Photonic integrated circuits (PICs) find application in many fields such as data communication networks and sensing [1]. However, the expensive photonic packaging is a barrier to the commercialization and application of PICs. The optical inputs and outputs (I/Os) are most challenging in photonic packaging because of the large mismatch of the optical mode size between a waveguide ($\sim 1 \times 1$ μm) and optical fiber ($\sim 10 \times 10$ μm), as well as tight alignment tolerances. Low-loss waveguide mode coupling requires sub-micron alignment accuracy which typically necessitates time-consuming active alignment[2]. Such alignment accuracies cannot be obtained even with high-end automated assembly machines that typically provide down to 2 μm placement accuracy. To overcome this problem one can use integrated spot-size converters (SSCs) on the InP or SiPH chip, to enlarge the mode in the waveguides to match that of the optical fiber and relax the alignment tolerance[2-5]. However, SSCs take up significant chip space and the minimum pitch limits the number of optical connections to less than 10 per mm which is insufficient for the trend of high optical port density in the next-generation data communication[6, 7].

In this paper, we present a passive alignment approach utilizing suspended waveguides based on TriPleX (SiN) technology, which has previously been demonstrated to interconnect densities of 40 per mm[8]. We apply this approach in a scalable and cost-effective photonic assembly concept. This process is targeted to deliver up to 112 optical I/Os which are self-aligned simultaneously during a flip-chip bonding.

Concept

The self-aligning structure connecting the InP chip to the TriPleX carrier consists of two parts: the suspended flexible waveguides on TriPleX and a triangular landing trench on

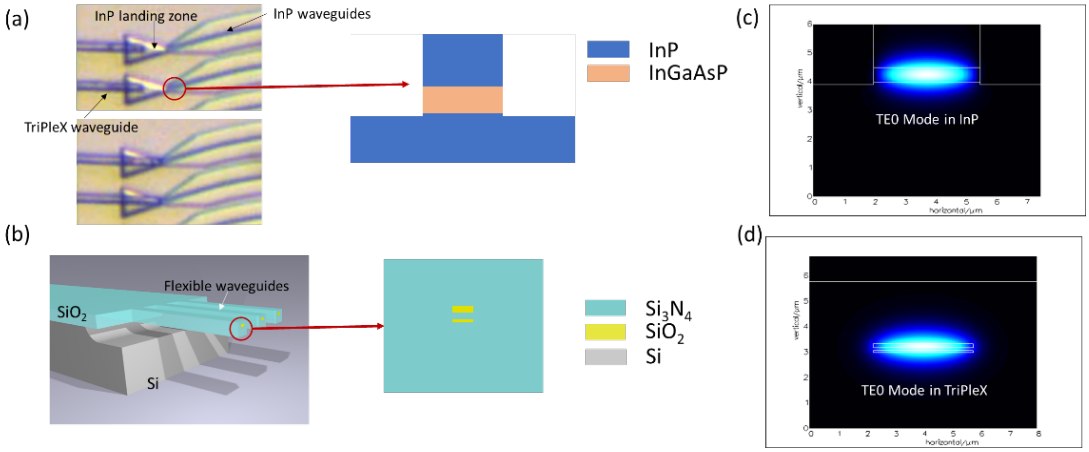

Figure 1: Schematic of flexible waveguides on TriPleX and their corresponding triangular landing trenches on InP. (a): Schematic of two types of triangular landing trenches ended with a straight and 7-degree angled lateral tapering waveguide on InP, the enlarged view is the cross-section of deeply-etch ridge waveguide geometry; (b): Schematic of 3 suspended waveguides, the enlarged view is the cross-section of asymmetric double-stripe (ADS) geometry. (part of the waveguides are omitted for simplicity); (c) and (d): Simulated optical fields (TE0) in a straight InP waveguide and a TriPleX ADS waveguide.

the InP chip that provides the mechanical guiding of the flexible finger to the correct position. This is shown in Figure 1 (a, b).

The landing trench on InP is in a triangular shape as shown in Figure 1a. There are two types: one connecting a straight waveguide and one connecting to a 7-degree-angled waveguide. The 7-degree-angle (as shown in Figure 1a) is chosen for minimizing the reflection. The enlarged view shows the cross-section of a deeply etched ridge waveguide. Figure 1b depicts a schematic of the TriPleX finger waveguide[9]. The waveguides are released and suspended by locally etching away the substrate during fabrication. The suspended waveguides are 500-750 µm long. The cross-section of flexible waveguides is in an asymmetric double-stripe (ADS) geometry that consists of two stripes of silicon nitride (Si_3N_4) on top of each other, separated by an intermediate 100 nm silicon oxide (SiO_2) layer as shown in Figure 1(b). The thickness for the upper Si_3N_4 stripe is 175 nm and the lower one is 75 nm. The waveguide geometry is offered within the standard TriPleX platform and is designed for coupling to and from optical fiber arrays with low loss by the integration of SSCs [9].

Simulation results

The TripleX and InP waveguides at the location of the triangular trench were simulated in Photon Design's FIMMWAVE and FIMMPROP software. The modes of both were designed to be matching by tailoring the waveguide geometry through adiabatic tapering sections. The coupling efficiency of the self-aligned structure depends on the geometries of the tips of the flexible waveguides and the triangular trenches, which is determined by fabrication tolerances.

Figures 1c and 1d depict the simulated optical fields of the fundamental TE mode of both whose mode field diameters are 2.7 µm (Δx, in-plane) and 0.9 µm (Δy, out-of-plane direction). To study the feasibility of the fabrication processes, the coupling efficiency is investigated by calculating the overlap integral between those modes as a function of the misalignment in vertical and lateral directions. Figure 2a presents simulated mode overlap integral as a function of misalignment in lateral (Δx, in-plane), vertical (Δy, out-of-plane) directions from 0 µm to 1 µm. Note that the vertical alignment is critical.

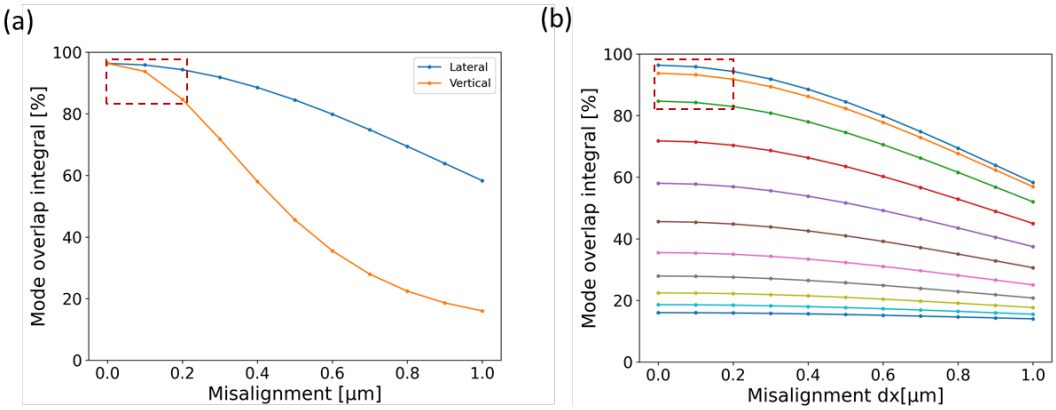

Figure 2: Simulation results: (a): Mode overlap integral versus lateral (Δx) or vertical (Δy) misalignment; (b): Mode overlap integral versus the product of misalignments in both lateral and vertical directions, each curve from top to bottom represents the mode overlap for a vertical misalignment from 0 to 1 μm at a 100nm step.

Figure 2b shows the total mode overlap integral as a function of the product of misalignments in both lateral and vertical directions. In this figure, each curve, from top to bottom, represents the mode overlap of a vertical misalignment from 0 to 1 μm at a 100 nm step.

With high-resolution fabrication, the alignment difficulty can be shifted to fabrication tolerance, by using the flexible waveguides. The coupling efficiency then depends on the fabrication tolerance of waveguide geometries. Since the fabrication tolerance of the high-resolution lithography is less than 200 nm, more than 80% mode overlap can be achieved, indicating a coupling loss below 1 dB.

Assembly concept

The self-alignment approach is applied in a hybrid assembly concept, as shown in Figure 3. We standardize on-chip dimensions and connections, including up to 112 optical interconnects and 58 electrical interconnects. The detailed standardized parameters can be found in [10]. The standardization allows us to reuse various parts and to focus on the functional and operational process, without limiting the applications space. A TriPleX carrier acts as an interposer that provides the optical interfaces to an InP PIC. One side of the waveguides on the TriPleX carrier connects to a standard optical fiber-array, the other side is self-aligned to the InP PIC. In addition, the TriPleX carrier provides the electrical interfaces to the InP PIC, which can be used for electrical probing and bonding to external electronic circuitry. Solder bumps are on top of the bonding pads which is fluxless Eutectic Gold-Tin (AuSn) with an 80-20 weight composition.

During the assembly, the InP PIC is flipped and moved to the pre-defined location by an automated pick-and-place machine. The PIC and carrier can be joined together by heating up the AuSn solder bumps locally by leveraging laser soldering technology. After the electrical connections are soldered, the InP chip is in position and the 112 optical I/Os are self-aligned to the waveguides on the TriPleX carrier. Shear force tests are performed afterward to check solder joint performance. Figure 3c shows that the maximum shear force is 6 N, which indicates a strong contact.

External fiber-arrays provide the connections to the TriPleX carrier. They are attached with established assembly processes, since the TriPleX waveguides at the edge of the carrier are mode-matched to standard single-mode fibers.

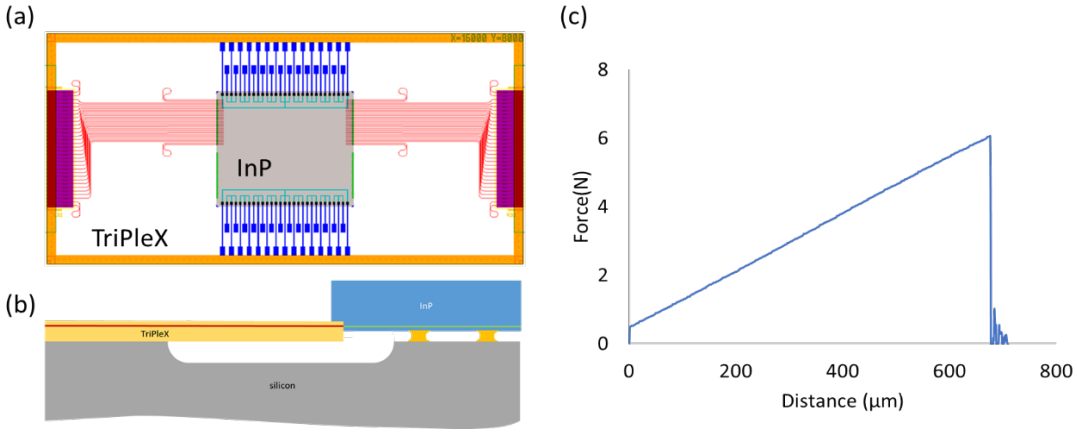

Figure 3: Schematic of a flip-chip assembled InP PIC on a TriPleX carrier. (a): the mask layout of TriPleX carrier and InP PIC with optical and electrical interconnects; (b): Schematic of a self-aligned flexible TriPleX waveguide to its counterpart on the InP PIC after flip-chip bonding; (c): Shear force test results of electrical interconnects.

Conclusion

In this paper, we presented the design of a self-aligned optical interconnect from fiber arrays to waveguides on an InP PIC. The concept is described and simulated, and critical elements are being experimentally investigated. This multiport assembly process promises to provide a scalable and cost-effective way for connecting a large number of optical and electrical ports to a photonic integrated circuit.

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