Micro-Transfer-Printed III-V-on-Si Semiconductor Optical Amplifiers with High Saturation Power

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Abstract

Integrated III-V-on-Si high saturation power semiconductor optical amplifiers (SOAs) with high output power are essential for silicon photonics (SiPh) as the leading candidate for high volume production of photonic integrated circuits (PICs) in a wide variety of applications and markets such as coherent optical communications, sensing and spectroscopy, and LiDAR. InP-based SOAs with high optical confinement can suffer from two-photon absorption and non-linear absorption associated with the generated carriers, while in this work, we used pre-fabricated InP SOAs, micro-transfer-printed (µTP) on a silicon waveguide within a silicon-on-insulator (SOI) PIC. The hybrid III-V/Si optical mode reduces confinement in the active region of the SOA, which results in an increased saturation power. The possibility of co-integration of high saturation power SOAs with the previously demonstrated µTP narrow linewidth widely tunable III-V-on-silicon lasers as optical output power boosters can lead to the required high output power of coherent optical communications. At the conference, we will present further details on the design, fabrication, and characterization results of the SOAs.

Introduction

SiPh realizes PICs on 200 mm or 300 mm SOI wafers with high uniformity and yield by taking advantage of the existing CMOS fabrication infrastructure. Since optical gain cannot be provided by Si, III-V semiconductors have been introduced to SiPh. The integration of III-V-on-Si high output saturation power SOAs is a must for SiPh to be the leading platform for high-volume applications such as optical communications, sensing and spectroscopy, LiDAR, etc.

In this work, the µTP method is used to integrate pre-fabricated InP SOAs [1] on a silicon waveguide within a SOI PIC. The SOA design relies on a hybrid III-V/Si optical mode [2], resulting in a reduced confinement in the active region, which has a narrow-to-wide tapered design, reducing power density towards the wide side of the SOA. This results in an increased output saturation power.

Design and Fabrication

There are two main approaches to achieve an integrated high output saturation power SOA [2]: 1- having low confinement in the active region, and 2- having a large cross-section active region.

As illustrated in Fig. 1(a), From left to right, the SOA consists of 4 sections: 1- a taper for evanescent partial coupling from single-mode Si waveguide to III-V, 2- a narrower side, which results in a higher gain for a given injection current, 3- a wider side, which provides lower power density, resulting in higher output saturation power, and 4- an inverted taper for coupling the light from III-V to the single-mode Si waveguide. The

SOA design relies on not only a hybrid III-V/Si mode to lower the confinement factor, but also a large cross-section active region in the widest part of its tapered design. The Si waveguide width underneath the III-V is consistently 2 µm wider than multi-quantum well (MQW) layers to keep the confinement in the active region low over all the fourth parts. Fig. 1(b) shows a stitched microscope image of the fabricated III-V coupon, which is µTP-ed on a Si waveguide within a SOI PIC.

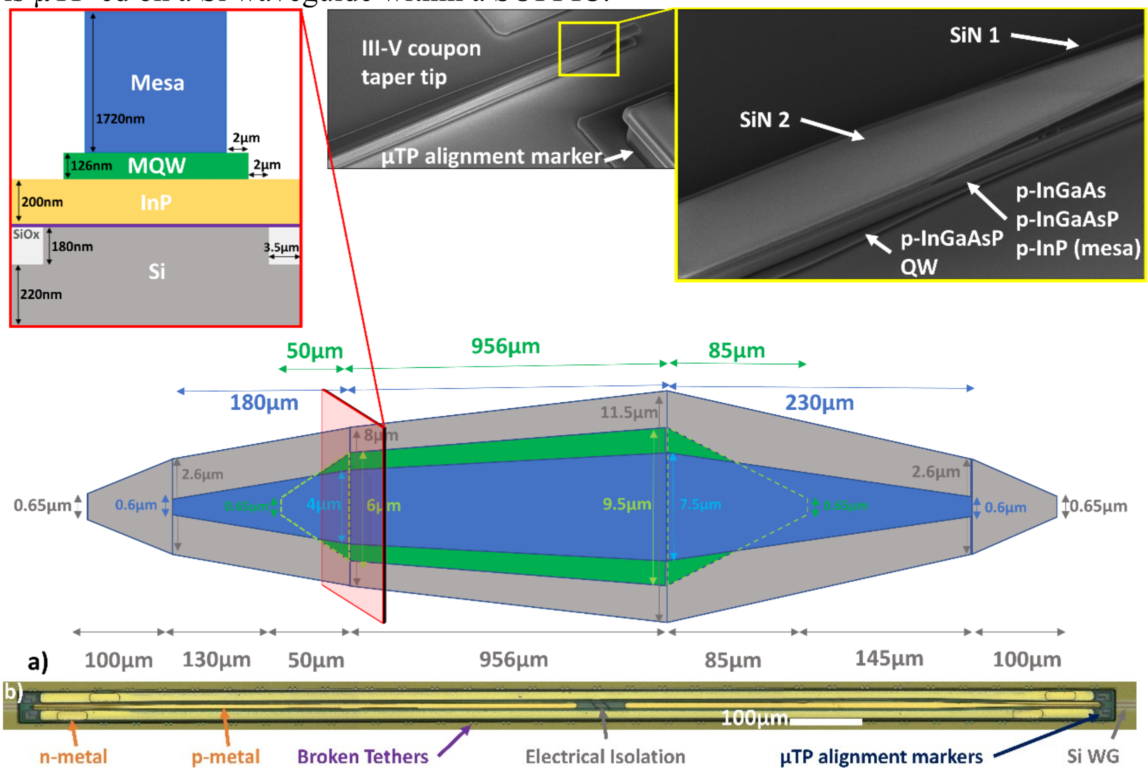

Figure 1: (a) Detailed schematic of the hybrid III-V-on-Si tapered SOA design (top view), indicating p-InP mesa, active area, and silicon waveguide underneath. A schematic cross-section and two SEM images of the III-V coupon are shown in the inset (not to scale), (b) Microscope image of a coupon µTP-ed on a Si waveguide.

In this work, we used a similar fabrication process flow and III-V epitaxial stack as the previously demonstrated µTP narrow linewidth widely tunable III-V-on-silicon lasers and transmitter [3, 4], which typically requires more quantum wells than high-output power amplifiers [5]. Here, there is just one additional step to create electrical isolation between the narrow and wide sides of the SOA by inductively coupled plasma (ICP) etching the 200 nm of cladding p-InP prior to p-metal deposition, in comparison to the described III-V fabrication process flow in [3]. The µTP process is based on the use of an elastomeric poly-dimethyl siloxane (PDMS) stamp to pick up the pre-fabricated InP-based SOA (which is undercut by selectively etching the release layer) from its native III-V source wafer and to print it on the target substrate, which contains 400 nm thick Si waveguides with an etch depth of 180 nm. A spin-coated DVS-BCB adhesive bonding layer of less than 40 nm enables a high-yield printing process.

Characterization

To characterize the SOA, the sample was placed on a 20°C temperature-controlled stage. The device under test is optically probed using cleaved standard single-mode fibers (SMFs) on a fiber stage. To have better control over the narrow side and the wide side of the SOA, which are electrically separated by the isolation island, separate probe needles are used to electrically drive each side of the amplifier, simultaneously. The left/right SOA section has a differential resistance of 11/9 Ω, while injecting 100 mA in each segment.

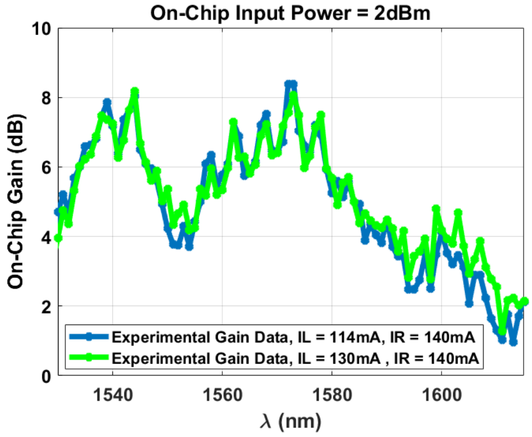

Figure 2: Gain as a function of wavelength, while the on-chip input power is +2.0 dBm and the pump current of the left and right sides are 114/130 mA and 140 mA, respectively.

The gain spectrum for 2 dBm optical input power is shown in Fig. 2, while the pump current on the left and right sides are 114/130 mA and 140 mA. The dip in the gain curves is attributed to the interference of two propagating modes in the SOA, which are excited by a slight misalignment of the transfer printed SOA. At the wavelength of 1544 nm and 1573 nm, which correspond to the wavelength of maximum optical gain for the left side pump current of 130 mA and 114 mA respectively, the small-signal gain of 8.4 dB and 9.4 dB and an output saturation power of 18.4 dBm and 15.4 dBm were extracted by fitting a curve to the experimental data according to (1), as shown in Fig. 3 and Fig. 4.

$$G(P_{in}) = G_0 \frac{1 + P_{in}/P_s}{1 + G_0 P_{in}/P_s} \tag{1}$$

Equation (1) relates the SOA gain factor G to the input power P_{in}, material gain saturation power P_s, and small-signal gain G_0 [2].

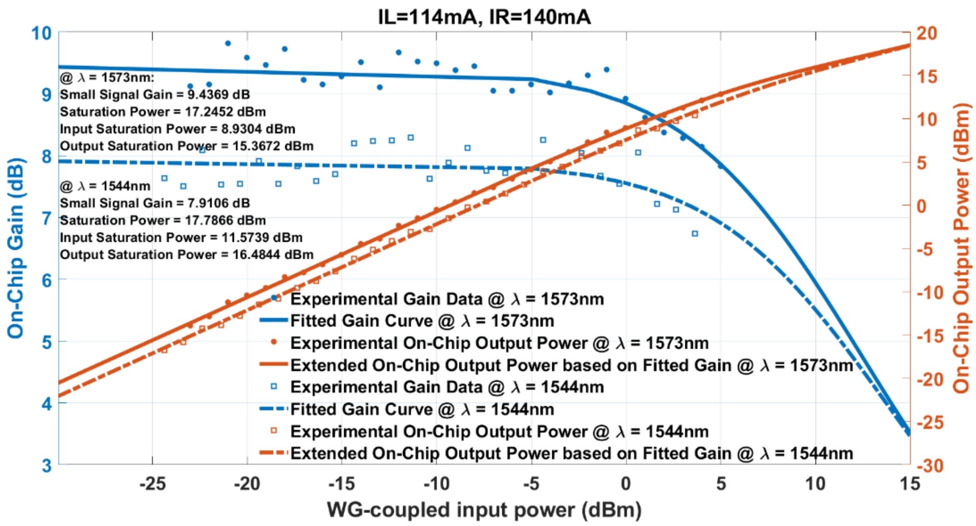

Figure 3: The gain as a function of on-chip optical input power (left side). The on-chip output power as a function of the input power (right side). The points are measured values and the lines are fitted curves at wavelengths of 1544 nm and 1573 nm. The pump current of the left and right sides are 114 mA and 140 mA, respectively.

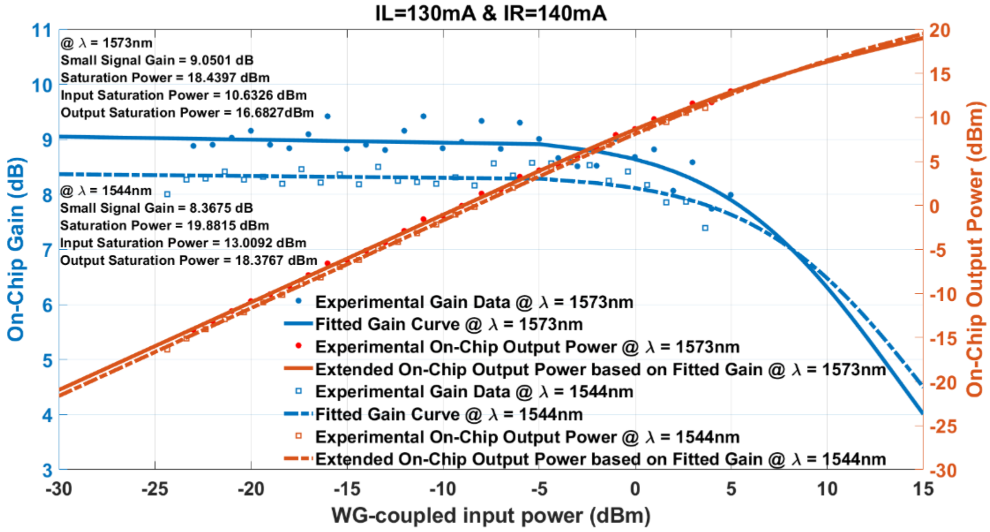

Figure 4: The gain as a function of on-chip optical input power (left side). The on-chip output power as a function of the input power (right side). The points are measured values and the lines are fitted curves at wavelengths of 1544 nm and 1573 nm. The pump current of the left and right sides are 130 mA and 140 mA, respectively.

Conclusion

We demonstrated a tapered µTP-ed III-V-on-Si SOA with an on-chip output saturation power of 18.4 dBm and an 8.4 dB small-signal gain at the wavelength of 1544 nm. µTP not only requires no singulation and handling of individual III-V chips, but also allows for densely integrating different non-native components on a SiPh platform with minimal disruption to the SiPh process flow in a high-throughput manner. The possibility of co-integration of the presented SOAs with the recently demonstrated µTP narrow linewidth widely tunable III-V-on-silicon lasers [3] and transmitter [4] as an optical output power booster, can lead to the required high output power for e.g. coherent optical communications.

Acknowledgments

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