# RF-choke for on-chip bias circuit monolithically integrated with high speed UTC-PD

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## Abstract

*This work reports on the monolithic integration of a bias circuit together with a high speed UTC-PD. The bias circuit consists of a coplanar waveguide line with a DC connection that is decoupled from the RF signal through a quarter wavelength stub. Two RF chokes are designed, for $K_a$- and V-band respectively, which are directly integrated with high speed UTC-PDs on an InP-Membrane On Silicon platform. S-parameter simulations demonstrate RF transmission losses below 3dB, reflections below -14dB and RF to DC isolation of 15dB over a range of 10GHz around the center frequencies of the two respective frequency bands.*

## Introduction

Although various bias-free uni-travelling carrier photodetectors (UTC-PDs) have been demonstrated [1]–[3], UTC-PDs generally demonstrate improved performance when a DC bias voltage is applied across the detector due to the increased internal electric field, which results in increased bandwidths and responsivities. When considering an integrated device to be used in commercial applications such as beyond-5G communications or microwave photonics, the photodetector should preferably be biased without the need of an external bias-tee, which can be achieved by an on-chip bias circuit. Such a circuit allows for separate DC and RF connections to interface with the UTC-PD. Although discrete component integration of a DC bias-tee with a UTC-PD can be used to achieve this [4], RF losses and impedance mismatches caused by wirebonds between the RF connections of the photodetector and bias-tee, as well as high costs from device assembly, can be avoided by monolithic integration [5].

This work reports on the monolithic integration of a bias circuit together with a high speed UTC-PD [6] in the nanophotonic InP-Membrane On Silicon (IMOS) platform [7]. Two circuits have been designed based on co-planar waveguide (CPW) RF chokes suitable for $K_a$-band (26.5–40GHz) and V-band (40–75GHz). The designs are numerically optimized to limit insertion loss, RF reflections and leakage from the RF to the DC path.

## Design

To provide a DC bias to the UTC-PD, an additional electrical path to the CPW line of the photodetector is required. For this design, a T-shaped connection is used to apply the DC bias to the RF path and thus to the UTC-PD. To prevent leakage of the RF signal towards the DC path, an RF filter is placed in the DC path, as can be seen in Fig. 1. The RF filter, or RF choke, consists of a quarter wavelength transformer leading to a virtual RF open circuit, blocking the RF signal to be passed through the DC line on the bias circuit [8, 9]. Capacitive decoupling of the RF line as present in a conventional bias-tee is not present in this design, which can however be added as part of external circuitry [8, 9]. The DC and RF CPW line parameters are optimized to have a 50Ω characteristic impedance and for compatibility with a commercial 110GHz RF probe with a 100µm pitch.

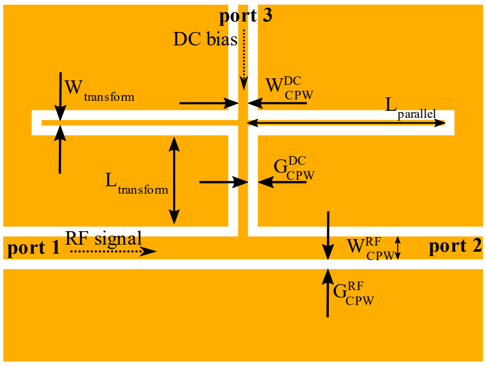

*Figure 1: RF choke based bias circuit*

*Table 1: Used material parameters*

| Material | $\epsilon_r$ | $h\ [\mu m]$ |
|---|---|---|
| BCB (bonding) | 2.5 | 1.8 |
| BCB (planarization) | 2.5 | 0.65 |
| $SiO_2$ (cladding) | 3.6 | 0.1 |
| Si (substrate) | 11.9 | 300 |
| Gold (bias circuit) | - | 0.4 |

All semiconductor layers used in the UTC-PD can be removed during the fabrication process. As a result, the bias circuit is designed based on a material stack consisting of a high resistivity 300µm thick silicon substrate, followed by a combination of $SiO_2$ and BCB layers. All relevant material parameters are listed in Table 1.

The design relies on out of phase reflections on the quarter wavelength section, which is inherently frequency dependent, so the design is optimized for a frequency range of interest. Therefore, two devices have been designed, suitable for $K_a$-band and V-band respectively. The length to the stub $L_{\mathrm{transform}}$ is designed to be match to the center frequency $f_0$, of the band of interest according to

$$L_{\mathrm{transform}} = \frac{c}{4f_0\sqrt{\epsilon_{\mathrm{eff}}}}. \quad (1)$$

The parameters $W_{\mathrm{transform}}, L_{\mathrm{parallel}}$ and $L_{\mathrm{transform}}$ (Fig. 1) have been numerically optimized to achieve the target performance specified in Table 2, where all goals have equal weight. CST Studio Suite was used for the numerical optimization and simulation of the devices.

*Table 2: Optimization targets and simulated results*

| Parameter | Numerical optimization target performance | Ka band results (30-40GHz) | V band results (60-70GHz) |
|---|---|---|---|
| $S_{12}$ (transmission) | > -1dB | > -3dB | > -3dB |
| $S_{11}$ (reflection) | < -12dB | < -14dB | < -18dB |
| $S_{13}$ (RF to DC leakage) | < -35dB | < -15dB | < -16dB |

## Simulation results

The obtained numerically optimized designs for both the $K_a$- and V-band circuits are simulated with increased accuracy using CST Studio Suite to obtain the S-parameters that directly give the RF transmission, RF reflections and RF to DC leakage. The simulation results for $K_a$- and V-band are provided as a solid line in Figures 2 and 3 respectively and show that not all target performance levels could be achieved simultaneously. The simulated transmission performance of both devices is limited to > -3dB and both the RF reflections and RF to DC isolation are limited to < -14dB. The results are also added to the overview in Table 2. In particular for the RF to DC isolation holds that there is an optimum band around the designed center frequency, which follows from the frequency dependent design according to Eq. 1.

Although the numerical optimization of the RF choke designs is not performed including the UTC-PD, the CST simulation of the final V-band design was extended with the addition of the UTC-PD and connecting metal tapers from the detector contacts to the RF-choke CPW lines. The results are added in Fig. 3 as a dashed line, and demonstrate a slight increase in transmission losses ($S_{12}$), as well as increased RF reflections across the full frequency range ($S_{11}$). The RF to DC isolation is slightly improved, but is in line with results excluding the photodetector. The differences are caused by the presence of a slight impedance mismatch between the UTC-PD and the bias circuit.

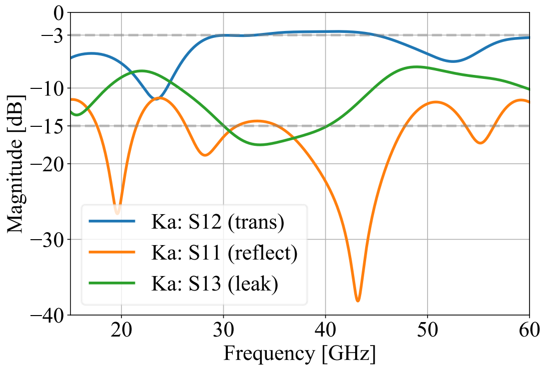


*Figure 2: Simulated S-parameters for Ka band*

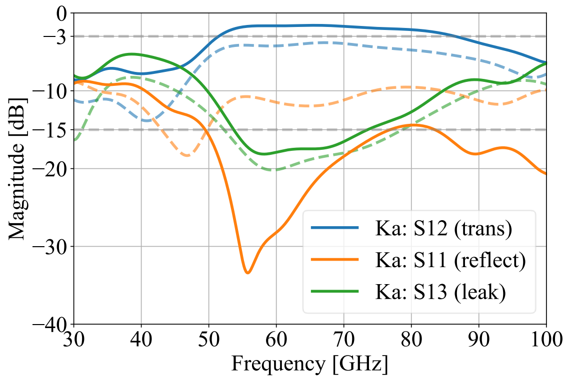


*Figure 3: Simulated S-parameters for V band*

## Fabrication

The final devices with a size of 1.5mm by 1.1mm for V band, and 2.5mm by 2.05mm for $K_a$ band were realized in the final metallization layer which connects to the p- and n-contacts of previously patterned UTC-PDs as can be seen in Figures 5 and 6. The wafer was planarized using BCB followed by an $SiO_2$ layer of 50nm to improve adhesion of the metal to the sample. The devices are fabricated by a metal lift-off step after patterning using electron beam lithography with PMMA resist. The metal stack consists of 50nm of titanium followed by 400nm of gold. Bias circuits are also fabricated without connections to a UTC-PD on the same wafer in order to characterize the devices individually.

Preliminary measurement results have confirmed electrical connection from the DC line to the UTC-PD enabling a DC bias to be applied. In future work, elaborate measurements using a vector network analyser will be carried out to determine the S-parameters of the devices.

## Conclusions

Monolithic integration of a bias circuit and UTC-PD can avoid losses, potential impedance mismatches caused by additional wirebonds as well as high costs from device fabrication and assembly, compared to discrete component integration. A bias circuit based on a CPW RF choke using a quarter wavelength RF filter in the DC line is designed based on first order approximations and numerical optimization for two frequency bands.

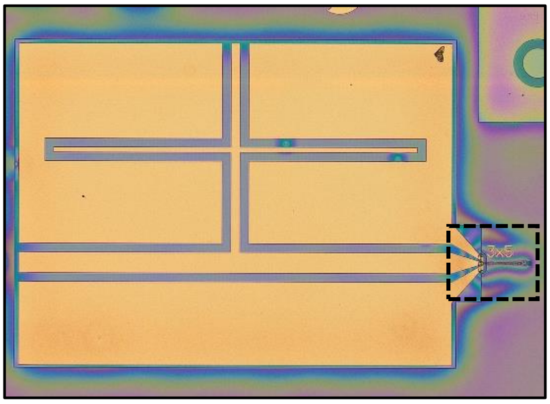

*Figure 5: V-band bias T integrated with UTC-PD*

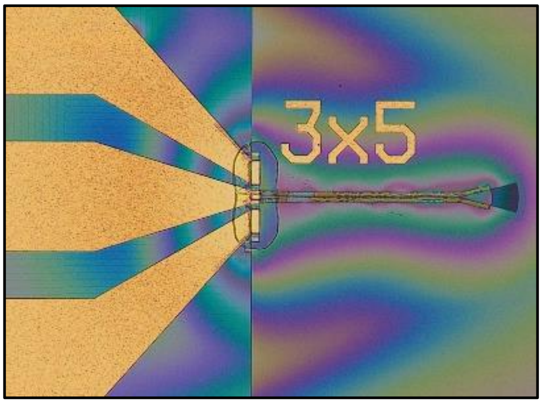


*Figure 6: V-band bias T integrated with UTC-PD (close up)*

Simulation results of two bias circuits designed for the IMOS platform for $K_a$- and V-band demonstrate insertion loss below 3dB, RF reflections below -14dB and RF to DC isolation of at least 15dB for a frequency range of 10GHz around the center of the respective frequency band. The optimized designs are fabricated in the final metallization step in the nanophotonic IMOS platform, and are monolithically integrated with high speed UTC-PDs. Preliminary measurements have confirmed the device ability to provide a DC bias to the UTC-PD, and future measurements on a vector network analyser have to be carried out to determine specific device characteristics.

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