Design and analysis of high-density SOA arrays on indium phosphide

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Applications such as optical switch matrices and optical phased arrays require many integrated components, e.g. semiconductor optical amplifiers (SOAs). We present a novel solution for increasing the density of SOAs using the open-mask regrowth technique which can eliminate the loading effect and growth rate enhancement which are typically seen for large-area or high-density active blocks. We designed SOA arrays using the proposed technique on a generic indium phosphide platform. In parallel, a systematic approach towards enabling transfer printing of SOA arrays on a single coupon is introduced. Thermal simulations of SOA arrays on a substrate and coupon show that arrays with several SOAs on a single coupon are possible with minor thermal penalty. Finally, the experimental plan on a generic indium phosphide platform is presented.

Introduction

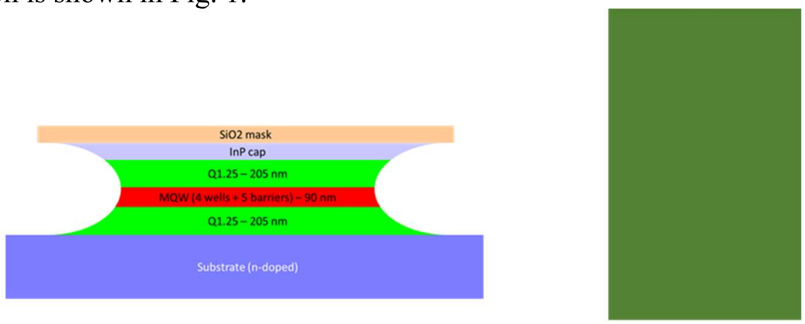
A monolithically integrated light amplification component is a key advantage of indium phosphide (InP) based photonic integration platforms. With the rapid developments of LiDAR and the ever-increasing bandwidth requirements for various applications, e.g. for optical switch matrices [1], neural networks [2] and programmable photonic circuits [3], the density on our optical chips is being pushed continuously. On integrated photonic platforms, the placement of highly dense SOA arrays can be challenging for several reasons, which can be categorized as optical, thermal, electrical and fabrication [4] limitations. For the scope of this paper, we will focus on the thermal and fabrication limitations of high-density arrays.

Micro-transfer-printing enables the integration of III-V coupons on silicon-based platforms [5], which combines the active components on the coupon with the low-loss silicon platform. In this paper, SOA arrays on InP substrates and InP coupons will be compared.

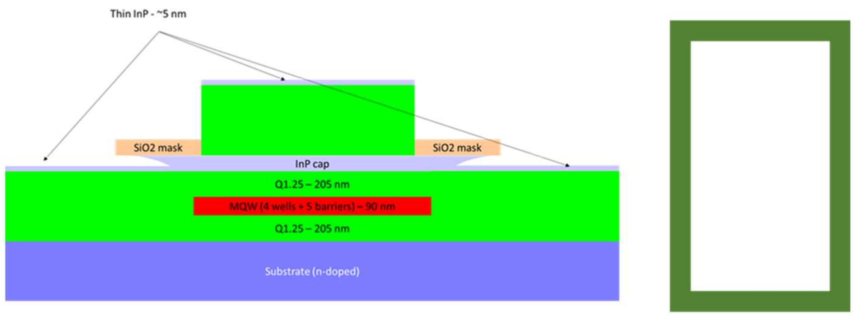
Fabrication challenges and solutions

On a typical InP integration platform, a regrowth step is carried out to define where the active and passive components are placed in the circuit. When placing SOA building blocks in dense arrays, one runs into issues with the regrowth of the passive layers, due to an effect called growth rate enhancement (GRE). This GRE appears when SOA arrays are densely spaced, which is named the loading effect, or when the active area that is covered during the regrowth process is too large [6]. These effects can cause issues in the butt-joint connection between the SOAs and passive waveguides, which can lead to high coupling losses and reflections.

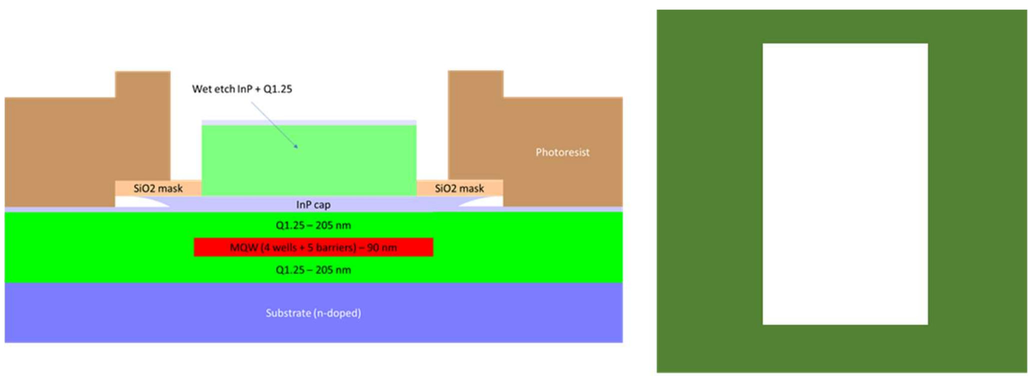
To avoid the GRE effect, an improvement to the regrowth process is proposed. This method is introduced for the first time in [4], and utilizes a hollow-mask approach to prevent GRE around close to the active islands. As a result, the GRE is not impacted by the size of the active islands. To illustrate this solution, a schematic step-by-step view of this solution is shown in Fig. 1.



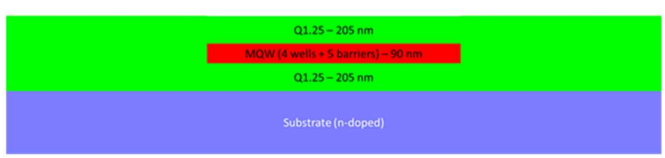
a) Masking and wet etching of active MQW core.



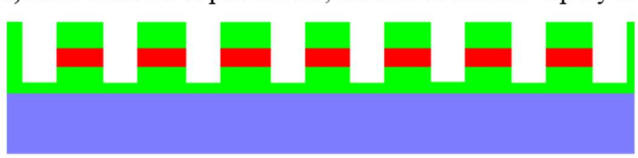
b) New hollow mask to allow growth on top of active areas.



c) Extra lithographic step to allow removal of overgrown material.



d) After removal of photoresist, hard mask and InP cap layer.



e) Patterned SOA array.

Figure 1 – Key steps of the hollow-mask regrowth scheme (not drawn to scale).

Thermal challenges and solutions

Placing multiple SOAs in a dense array, results in higher thermal crosstalk and a more challenging thermal management. We investigated the thermal performance of SOA arrays on InP substrates and transfer-printed coupons using commercial simulation software.

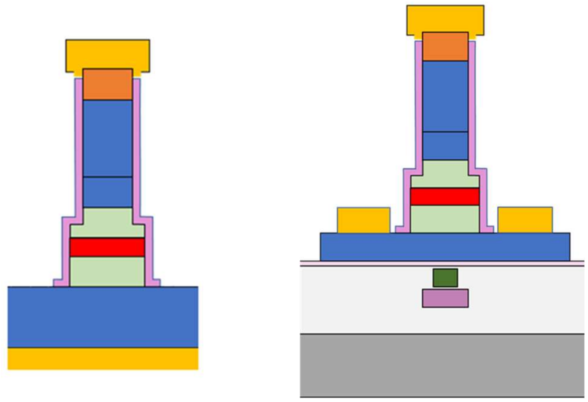


Figure 2 – Cross section of a monolithically integrated SOA (left) and micro-transfer-printed SOA (right).

For substrate based arrays and coupons, the cross section is shown in Fig. 2. Since the typical upper limit of a coupon width for micro-transfer-printing is around 100 µm, the pitch of the SOAs in the array has to be chosen carefully. The thermal input power for each SOA is chosen to be 100 mW for an SOA length of 500 µm, which is around the typical operating point. The output of the simulation provides the temperature increase in the SOA core, for each SOA in the array. We are showing the highest temperature reached in the array, typically of the center SOA. The temperature increase of substrate-based and transfer-printed SOAs is shown in Fig. 3.

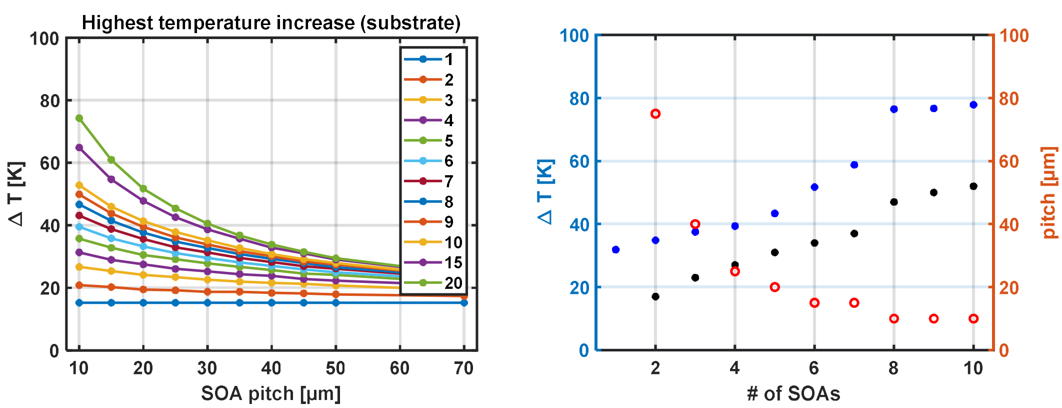


Figure 3 – The temperature increase in the center SOA of an array on substrate (left) and on a transfer-printed coupon (right). On the left ΔT is shown for various SOA pitches (x-axis) and number of SOAs in array (legend). On the right ΔT is shown for a 100 µm wide coupon with one to ten SOAs (x-axis) with optimized pitch. In black, the equivalent is shown for substrate-based arrays.

From the substrate-based figure, we can conclude that with a 70 µm pitch the thermal penalty is as low as 10°C up to arrays with 20 SOAs. When decreasing the pitch, the thermal penalty is increases as expected. The impact on the SOA performance is still to be experimentally investigated for transfer-printed SOAs.

The coupon-based arrays demonstrate a more dramatic impact. For example, if placing 10 SOAs with 10 µm pitch on a coupon, the thermal penalty is almost 80°C, where on a substrate this only gives a slightly over 50°C increase in temperature. In Fig. 3 (right) the increased thermal penalty of the coupon-based arrays with respect to the substrate-based ones can be observed. In this case, the pitch on the substrate is chosen equal to the pitch on the coupon. The increase in thermal penalty is between 12 and 32 degrees, depending on the number of SOAs in the array. The increase in thermal penalty from one to five SOAs on a single coupon is only slightly above 10°C, which indicates that up to this array size, the thermal penalty is expected to give acceptable SOA performance. An experimental plan to verify these simulations has been designed on both a monolithic InP and coupon-based platform.

Conclusion

In this paper, we present the main thermal challenges and fabrication challenges for making dense SOA arrays on InP substrates and transfer-printed coupons. Solutions to overcome these challenges have been presented, and supporting simulations are carried out to identify the possibilities on both platforms. An experimental plan is crafted to verify the novel regrowth strategy to enable dense SOA arrays on active-passive indium phosphide platforms, and to verify the simulated thermal behavior of dense arrays.

Acknowledgements

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