A Heat Sink for the Vertical Integration of InP Membrane Nanophotonic Devices on InP Electronics

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Abstract

In this paper, we study the thermal performance of Indium-Phosphide-membrane-on-Silicon (IMOS) semiconductor optical amplifier-based devices with/without heat sinking for standalone functionality on bare Si, and for vertical integration on top of InP high-speed electronic drivers. By implementing 5µm-thick Au heatsink, the thermal resistance was reduced by 2.56× to 0.0864 K.m/W compared with devices having no heat sink. Simulations matching the SOA design show the versatility of this heat sink for a wide range of BCB thicknesses 0.5-30µm. Implementing further improvements on the heat sink structure can reduce the thermal resistance by another ≈2×. Also from simulations, a thermal resistance value of 0.06658 K.m/W is expected for co-integrated devices.

INTRODUCTION:

Vertical integration of photonic devices with electronic driving circuits is one of the major milestones for the research on Photonic integrated circuits (PICs) [1]. This scheme enables tightly stacking and connecting photonic devices directly on top of electronic driver circuits at unprecedented distances below 20µm. It yields 3-dimentional monolithic circuits with improved electro-optic performance photonic devices, reduced energy consumption due to lower parasitic effects of long wires, and the possibility of high integration density for devices and interconnects. A promising photonics platform that is compatible with this integration scheme is the Indium Phosphide membrane photonics (IMOS) platform [2]. It consists of membrane-based active and passive devices bonded onto a substrate carrier with a Benzocyclobutene (BCB) polymer (InP-BCB-Si). These membrane devices are compatible for co-integration to both InP high-speed electronics and to BiCMOS drivers as well. However, one major challenge during fabrication here is the high surface topology of the electronics and photonics wafers, which requires using 10-16 µm-thick BCB to planarize these surfaces and achieve void-free bonding for the case of InP electronics [3]. This is exacerbated even more in the case of co-integration on BiCMOS drivers where 20µm BCB was required [4]. Thick BCB is suitable for lowering the thermal and optical interference between the two interfaces [5]. However, BCB thickness is crucial to the performance of photonics because of its very low thermal conductivity of 0.293 W/m/K, coupled with the fact that the thermo-electric cooler (TEC) can only be placed onto the InP DHBT substrate's backside. So active cooling is only achieved through the InP substrate. While the high thermal insulation of BCB is advantageous for low thermal interference between the photonics and electronics, the heat generated by the photonic devices needs to be efficiently dissipated down towards the substrate that is the only route to active cooling. Consequently, A comprehensive analysis of the thermal performance of IMOS devices and its compatibility with this integration scheme has not been yet investigated. Hence it is crucial to first address this point, and also to develop a reliable heat sinking strategy to dissipate the heat from photonics while being compatible with this co-integration scheme. This has been shown effective for many platforms [6], [7]

In this paper, we investigated the heating characteristics of semiconductor conductor amplifier- (SOA)-based structures on IMOS. There are key building blocks of this platform having high heat-sensitive performance. Thermal impedance (Z_{th}) was chosen as figure-of-merit to assess these characteristics. We performed fabrication-tolerance driven simulations for devices with and without a heat sink for a wide range of conditions spanning the full design space of the SOAs, and targeting both standalone functionality on Si as well as for the co-integration scheme.

The structure of the paper is as follows. First, we describe our experimental and simulation setup. Next, we assess the experimental and theoretical thermal impedance results of SOAs with heat sinking. We also compare simulation values of the designed SOAs with/without heat sink at various conditions. Finally, we discuss the effect of further improvements on the SOAs' heat sinking structure to its thermal impedance.

Simulation setup:

The simulation setup is designed according to the exact geometry of the SOAs with/without heat sinking. Fig.2.a) shows the setup for SOAs with heat sinking. A zoomed up view of the SOA core structure is shown in Fig.2.b), matching exactly the grown epitaxial stack and geometry of real SOAs. Fig.2.c) shows the setup for SOAs with no heat sinking. The heat is mainly generated by the SOA active core, so the red region in Fig.2.b) is set as the heat source for simulations. A heatsinking temperature of 300K is set at the bottom of the Si substrate, while the top surfaces are set to natural convective cooling in air environment at room temperature with heat transfer coefficient h=5 $W/m^2/K$. The two side boundaries are set to be isolating in order to restrict the heat to the real SOA pitch.

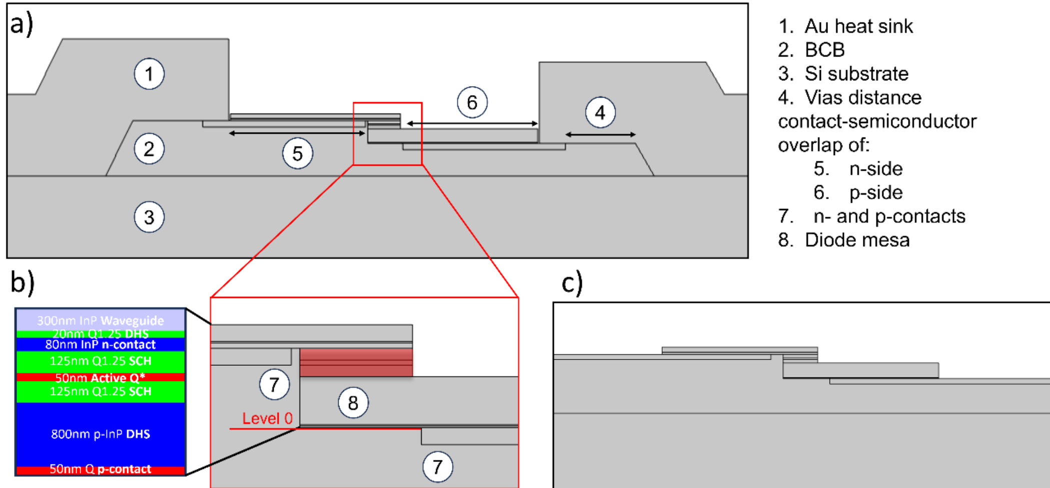

Fig.2. Simulation geometry of: a)SOAs with heat sinking, b) zoomed up view of the SOA core, showing the heat source, c) standard SOAs on IMOS

As for the selection of simulation parameters shown in Fig.2 and their variation range, these simulations were tailored to match the possible fabrication scope. For this, the Au heat sink (1) thickness values span a wide range of 0.2-5 µm, considering it can be fabricated with both lift-off or electroplating. The investigated BCB thickness (2) range is 0.5-30 µm, with lower limits representing demonstrated IMOS devices, while higher values are more compatible with vertical integration of the platform on top of electronics. The BCB thickness is defined with respect to level 0 shown in Fig.2.b), which matches the design thickness of BCB after bonding since it represents the majority of the wafer area. The Si substrate (3) extends downward to 300µm thickness for the standard setup, and a range of 100-600µm to investigate the substrate effect. InP and SiC substrates were also investigated using a thickness of 300µm for comparison. Vias distances (4) of 1 and 6µm were investigated, with the latter corresponding to the real fabricated devices. For (5 and 6), The n- and p-metal-contact-semiconductor overlap widths are both set to 7 and 2 µm, while 7µm is used in real fabrication 2µm corresponds to the lowest possible value for efficient current injection into the diode considering the specific contact resistance of InGaAs-based contacts on III-V layers. The initial n- and p-contact thickness (7) is 0.3 µm, which corresponds to the Ni/Ge/Au and Ti/Ge/Au contacts on the n- and p-sides, respectively, a thickness of 0.5 µm was also investigated since it can be realized in the same lift-off step. Finally, mesa widths (8) of 2 and 1 µm were investigated, with the former being the standard value. We note that all of the interfaces on the two ends of the structures in Fig.2.a) and Fig.2.c) extend to the entire SOA pitch with a chosen value of 200µm.

For analysis, the maximum temperature of the active core is extracted for different input powers. The simulated thermal impedance (Z_{sim}) is calculated as:

$$Z_{sim} = \frac{\Delta T}{\Delta P}$$

Where ΔT is the temperature difference corresponding to the difference in power ΔP.

Experimental setup:

To measure the thermal impedance of IMOS SOAs, we fabricated distributed feedback lasers (DFBs) on a run based on bulk active material with epi-stack shown in Fig.2.b). DFBs are ideal for stable single mode operation, which is required to track the lasing wavelength for different conditions [7]. The fabrication of

standard SOAs based on twin-guide architecture is described in [2]. Heat sink fabrication is introduced after bonding and in the last 3 last steps, where the BCB is opened near contacts and 5µm-thick gold is electroplated to connect the p- and n-contacts of the diode with the Si substrate. Schematics of both SOA types are shown in Fig.2. Both SOAs with/without heatsink are fabricated in the same run. The experimentally-obtained thermal impedance (Z_{exp}) can be calculated using:

$$Z_{exp} = \frac{d\lambda}{dP} / \frac{d\lambda}{dT}$$

Where $\frac{d\lambda}{dP}$ is the optical mode's wavelength shift in continuous operation (DC) at a constant temperature, while $\frac{d\lambda}{dT}$ is mode's wavelength shift in pulsed operation (AC) at varying temperature. Here, the pulse width is 200ns at a frequency of 1kHz to guarantee no self-heating with high pulse definition. Z_{sim} and Z_{exp} values can be normalized by multiplying it with the SOA length. The latter is referred to as thermal resistance.

Improvement of heat dissipation in IMOS SOAs using a 5µm-thick Au heatsink:
Fig.3.a) shows the cross-section of the fabricated SOA with heat sinking on both contacts. The superimposed thermal profile is from a simulated structure with identical geometry to the fabricated SOA at a current injection of 4kA/cm^2 for a 750µm long SOA. Fig.3.b and Fig.3.c) correspond to the AC and DC measurement results of a 750µm DFB with identical structure to the SOA shown in Fig.3.a), respectively. The thermal profile of a standard IMOS SOA with no heat sink at identical conditions to Fig.3.a) is shown in Fig.3.d).

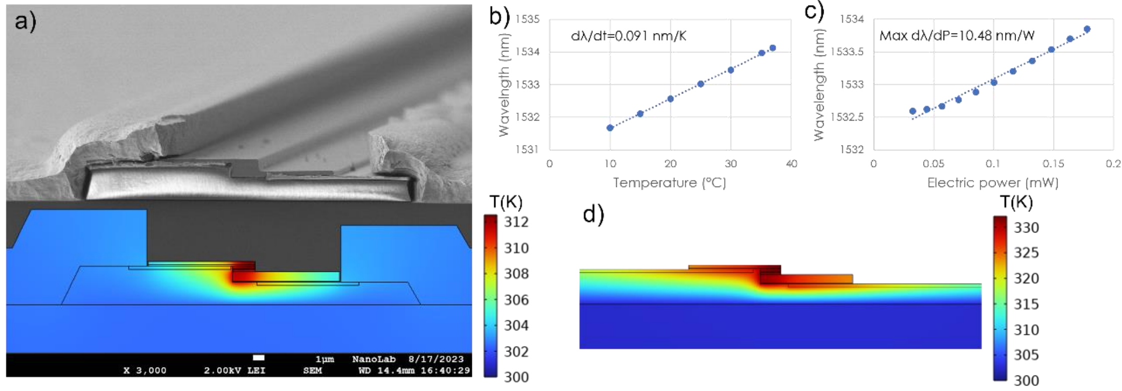

Fig.3. a) SEM cross-section of the fabricated SOA superimposed with corresponding simulated thermal profile for a 750µm SOA at current injection of 4kA/cm^2. b) peak wavelength of the 750µm DFB: b) *vs* TEC temperature in pulsed mode. c) *vs* input electric power in DC. d) thermal profile of a standard 750µm SOA with no vias at current injection of 4kA/cm^2

After fitting, the extracted DFB wavelength shifts from AC and DC measurements are: dλ/dt=0.091 nm/K and dλ/dP=10.48 nm/W, respectively. This yield Z_{exp} value of 115.16 K/W for the 750µm DFB, *i.e.*, a thermal resistance of 0.0864 K.m/W. This value is higher than state-of-the-art heterogeneously integrated III-V based photonic devices, with experimentally demonstrated values between 0.03-0.05 K.m/W [8]. However, these devices are integrated on the die scale and on thinned substrate holders as well. Nonetheless, it is possible to further improve the heat sink performance by bringing the thick Au closer to the hot spot region (active core) without compromising on the optical losses. These improvements are discussed in the next sections based on real fabrication tolerances. From simulation, the thermal resistance of this SOA is 0.0815 K.m/W which is 5.6% smaller than the measured value. However, the simulated thermal resistance of the standard SOA with no heat sink yield a value of 0.2088 K.m/W, pointing to a ≈2.56× improvement in thermal resistance using this heat sinking scheme.

Effect of BCB thickness on the thermal impedance of SOAs:
Fig.4.a) shows Z_{sim} values of a 500µm SOA with/without heatsink at different BCB thicknesses. Z_{sim} values of devices with no heat sink increase drastically at semi-linear rate *vs* BCB thickness. For instance, Z_{sim} for the standard IMOS thickness of 2µm is ≈417 K/W. This value is 893 K/W for BCB thickness of 10µm, which is the minimum thickness required for co-integration with electronics. The corresponding

profiles to these configurations are shown in Fig.4.b) and Fig.4.c). The increase of Z_{sim} for devices with heat sink *vs* BCB thickness depends mainly on the heatsink thickness. Using 200nm Au is not sufficient for dissipating the heat towards the substrate where Z_{sim} can increases from 277K/W to 434K/W with BCB thickness increase from 2 to 10µm. Using thicker Au heatsinks allows for better heat dissipation, where Z_{sim} increases by only by ≈30K/W for 1µm-thick vias, and by <10K/W for 2.5 and 5µm-thick vias, if BCB thickness is increased from 2 to 10µm. The thermal profiles of devices with 5µm Au at these BCB thicknesses are shown in Fig.4.d) and Fig.4.e). This highlights that a similar thermal performance of devices with heatsink thickness >2.5µm can be expected in the co-integration case compared to the case where devices were measured. Moreover, the thermal impedance here is mainly dominated by how well the heat sink can extract the heat from the SOA core directly, which necessitates further improvements to the heat sink structure as well as using active materials that are more tolerant to heat variation, for instance Al-based III-V materials.

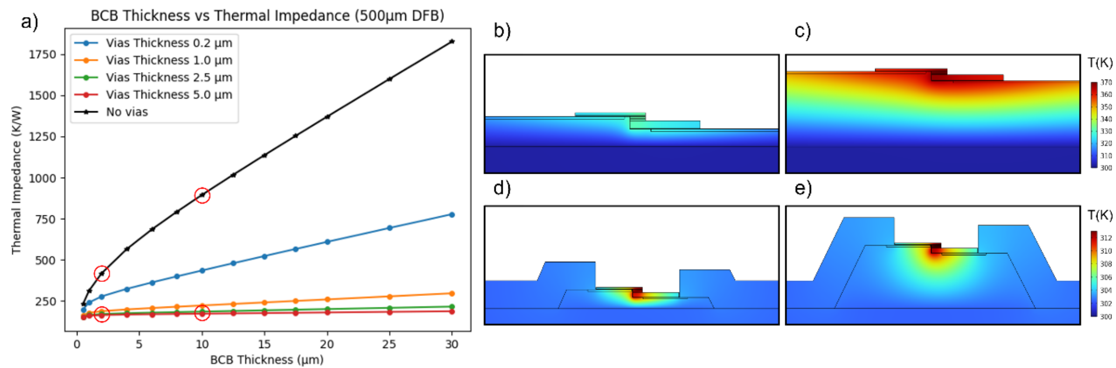

Fig.4. a) Simulated thermal impedance values for 500µm long SOAs with/without heatsink for different BCB thicknesses, profiles of highlighted points are shown in b-e. Thermal profile of: a standard SOA at b)2µm and c)10µm BCB thickness, SOA with 5µm heat sinks at d) 2µm and e) 10µm BCB thickness.

Effect of further improvements to the heat sink and SOA geometry on its thermal performance:
Fig.6 shows the effect of several improvements of the overall structure on Z_{sim}. From Fig.6.a), using 200 nm thicker gold for initial contacts is only beneficial for devices with no heat sink. This is because thicker gold helps in spreading the heat to the sides of SOA, while for SOAs with heat sink, having thick Au nullifies this effect. This finding is also consistent with the effect of pitch shown previously. We note that a reduction of ≈15% in thermal impedance of standard IMOS devices can be achieved following this improvement. The effect of substrate thickness is shown in Fig.6.b). A reduction of Z_{sim} by≈20K/W can be achieved for each 100µm reduced in Si substrate thickness. This is because heat mainly dissipates through substrate. Moreover, for all configurations, using InP substrates imposes ≈35 K/W higher Z_{sim} relative to Si, while using SiC substrates reduces Z_{sim} by ≈25 K/W relative to Si, which are linked to the thermal conductivity difference between these substrates.
The vias structure can also be improved. Fig.6.c) shows the potential impact of shifting the vias sloped region 5µm closer to the initial SOA metals. However, this improvement is only beneficial for vias thicknesses below 1µm. Fig.6.d) shows the impact of etching the doped semiconductors closer to the mesa, i,e, lower n- and p-metal-semiconductor overlap. This improvement is much more important for thick vias >1µm. Here, the thermal impedance can be lowered by an additional ≈25% for all BCB thicknesses.
Implementing these improvements, the thermal resistance of standalone devices at 2µm BCB can be reduced to 0.0443 K.m/W without influencing the optical losses of the diode, which is in the range of state-of-the-art heterogeneous devices. Moreover, from these simulation, the calculated the thermal resistance of co-integrated devices bonded onto InP with 10µm BCB using these optimizations is 0.06658 K.m/W, which validates the possibility of this co-integration scheme from a thermal perspective. We also note that simulations with mesa width of 1µm show the same thermal impedance values discussed here. Using thinner mesas can lower the power consumption of the overall diode, but can negatively impact its gain and saturation power. However, it might be possible to further improve the SOA thermal behavior by using thinner SOAs with an optimal compromise between these effects.

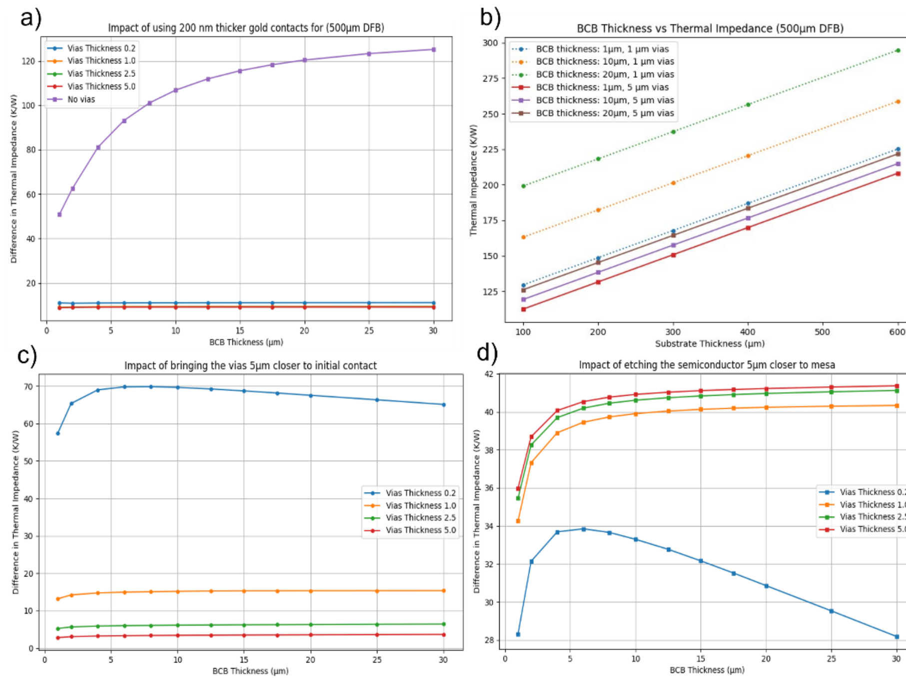

Fig.6. Simulated thermal impedance reduction for 500µm long SOAs with/without heatsink showing impact of: a) using thicker contact Au *vs* BCB thickness, b) substrate thickness, c) shifting the vias closer to initial contact, d) contact-semiconductor overlap width

CONCLUSION:

In this study, we investigated the thermal performance of IMOS SOAs, both with and without heat sinking, for standalone functionality and for 3D integration with electronics. The introduction of a 5µm-thick Au heat sink resulted in a reduction in thermal resistance by 2.56× compared to SOAs with no heatsink, with measured value of 0.0864 K.m/W. Our simulations demonstrated the versatility of this heat sink across a broad range of BCB thicknesses spanning 0.5µm to 30µm. Further enhancements to the heat sink structure hold the potential to reduce thermal resistance by another ≈2×. Additionally, the expected thermal resistance of co-integrated devices on InP with 10µm BCB is 0.06658 K.m/W, which holds promise from this integration scheme.

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