Monolithically integrated balanced photodiodes on InP

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We present a monolithically integrated InP balanced photodetector fabricated by introducing additional process steps into the standard platform of SMART Photonics. This overcomes an otherwise inevitable electrical connection between the diodes in the detector. The process steps and the characterization results from fabricated balanced photodetectors are presented.

Introduction

In coherent optical communication systems designed for high spectral efficiency and high baud rates, balanced detectors play a crucial role in mitigating both the laser relative intensity noise and the ASE noise stemming from in-line amplification [1]. They are also one of the key components of receivers in CV QKD [2], enabling shot noise-limited quadrature measurements on low power signals.

Previously, monolithically integrated pin-photodetectors on platforms such as InP [3], Germanium-on-Silicon [4], Silicon-on-Insulator [5], and monolithically integrated InGaAsP uni-travelling carrier photodetectors [6], as well as hybrid flip-chip integrated balanced photodetectors [7] have been demonstrated.

In this work, we report on balanced photodetectors (PDs) fabricated by introducing additional steps on the generic InP integration process of SMART Photonics. The shared n-doped ground plane across the photonic circuit, and the shared p-doped top cladding layer in the standard process result in parasitic electrical connections, preventing fabrication of photodetectors in balanced configuration. We explain the developed extension in order to overcome this limitation and present the characterization results from the fabricated balanced photodetectors.

Fabrication

The cross-sections used in the fabricated balanced PD are shown in Figure below. The active and passive cross-sections are separately grown and butt-jointed on a semi-insulating (SI) InP wafer [8]. The passive waveguide (WG) cross-section shown in Figure 1(a) is made up of InGaAsP quaternary waveguiding material (Q1.25), sandwiched between a p-doped InP cladding layer on top, and an n-doped InP cladding layer at the bottom. The pin-photodetectors have an active WG cross-section (as shown in (b), with a multi-quantum-well inside the WG layer, and a p-contact metal on top to collect the generated photocurrent. Optical access to photodetectors is provided by butt-joined passive WGs.

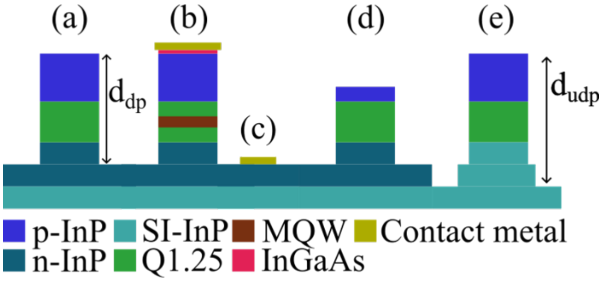

Figure 1 – The cross-sections used in the fabricated balanced PDs

In a conventional balanced detector configuration as shown in Figure 2(a), two photodiodes are serially connected where the cathode of one photodiode is connected to the anode of the other. The output current of the balanced detector I_{out} is equal to the difference of the individual photocurrents I_{PD1} and I_{PD2}. A balanced detector is typically followed by a trans-impedance amplifier. Considering the WG cross-section of the generic process flow where the conductive n-doped layer under the waveguiding layer extends across the die; placing two photodiodes on the same chip will result in parasitic connections with resistances of <1kΩ between their cathodes through the conductive n-doped layer. If the WGs coupled to the photodiode pair are not crossing or are not joined via passive couplers/splitters in a circuit, the parasitic connection can be eliminated simply by etching a trench through the n-InP layer, into the SI-InP, between the diodes and thus electrically isolating them.

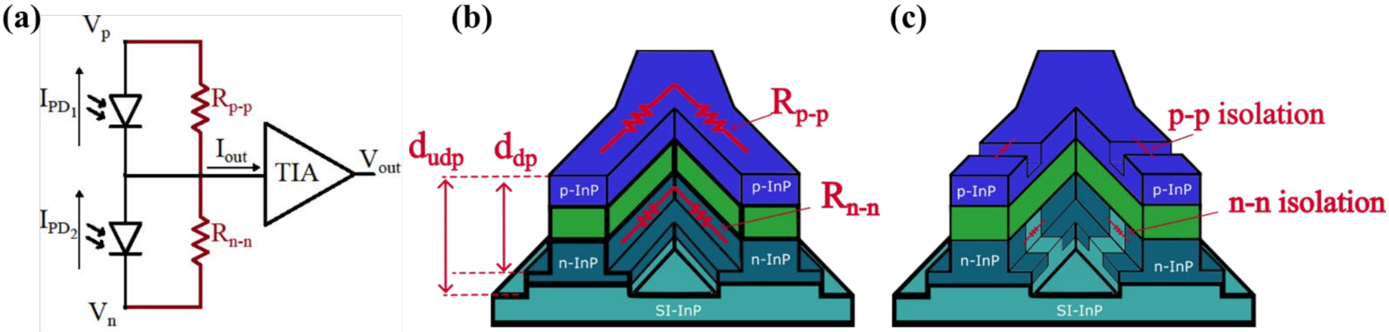

Figure 2 – (a) Circuit diagram of the balanced photodetector followed by a TIA (b) An example schematic of parasitic connections through n-InP and p-InP layers at a Y-junction (c) Schematic with introduced p-p and n-n isolation sections

However, the balanced photodiodes are usually accompanied by on-chip optical couplers/mixers in classical/quantum communication receivers. An example 3-D schematic of a connection of two WGs via a Y-junction is shown in Figure 2(b). Having the WGs leading to the photodiodes coupled to the same passive device results in electrical connections between the cathodes of the PDs (shown with R_{n-n}) through the conductive n-InP layer under the WG, and between the anodes of PDs (shown with R_{p-p}) through the p-doped layer over the WG.

These connections act as parallel current paths for the I_{out}, reducing the trans-impedance gain significantly as their resistance becomes comparable to the input impedance of the TIA in the small-signal regime. Furthermore, when a certain DC reverse bias is applied between V_p and V_n, the mismatch between R_{n-n} and R_{p-p} will result in an imbalance on the individual voltage drop across each PD, preventing controlling the voltage drop on individual photodiodes, and consecutively causing a DC current to flow into the TIA due to the mismatch of diode currents under different bias. An additional resistive circuitry can be included in the TIA to assist in controlling their voltage drop, as well as preventing the current flow into the TIA, provided the values of R_{n-n} and R_{p-p} are high enough so that the resulting circuitry does not further compress the TIA gain.

The generic process flow allows placing an electrical isolation section on WGs with a cross-section as shown in Figure 1(d) and Figure 2(c), named as "p-p isolation", enabling to increase the resistance R_{p-p} to MΩ level. With a goal of breaking the electrical connection through the n-doped layer under the WGs while keeping the optical functionality unaffected, a third cross-section with a layer stack where the n-doped layer is replaced with a semi-insulating InP layer, as shown in Figure 1(e) and Figure 2(c), named as "n-n isolation", is introduced. The newly introduced layer stack is fabricated by including the additional steps of etching away the SI wafer anywhere except where the n-n isolation cross-section is desired, followed by an extra epitaxial n-InP growth prior to the active-passive regrowth in the standard generic process flow.

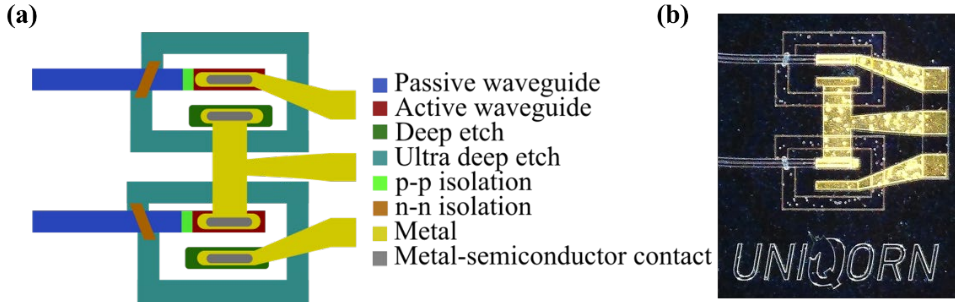

Figure 3 – (a) Top view drawing of the balanced photodetector layout.

Figure 3(a) shows a drawing of the balanced photodetector placed on the chip with the corresponding isolation cross-sections. The active WGs are encircled by an ultra-deep etched trench with an etch depth of d_{udp}. Where the WGs are crossing this trench, the passive WGs leading up to the active WGs are replaced with the n-n isolated waveguide cross-section shown in Figure 1(e). The p-p isolation section is placed right before the passive-active WG interface. The p-contacts are applied on top of the active WGs, and the n-contacts are applied to the deep-etched sections with an etch depth of d_{udp}. The connections are routed to the metal pads with a ground-signal-ground (GSG) configuration next to the balanced PD. Figure 3(b) shows a microscope image of the fabricated balanced PD.

Characterization results

Figure 4(a) illustrates current-voltage (IV) scans for individual PDs. The recorded dark currents are at 8.2 μA and 22.6 μA at −5V for PD_1 and PD_2, respectively. In Figure 4(b), the IV scans are presented in a linear scale around 0V. The calculation of slope near the zero-bias point yields parallel resistances of 1.71 MΩ and 130 kΩ for PD_1 and PD_2, respectively, which we attribute to $R_{p\text{-}p}$ and $R_{n\text{-}n}$.

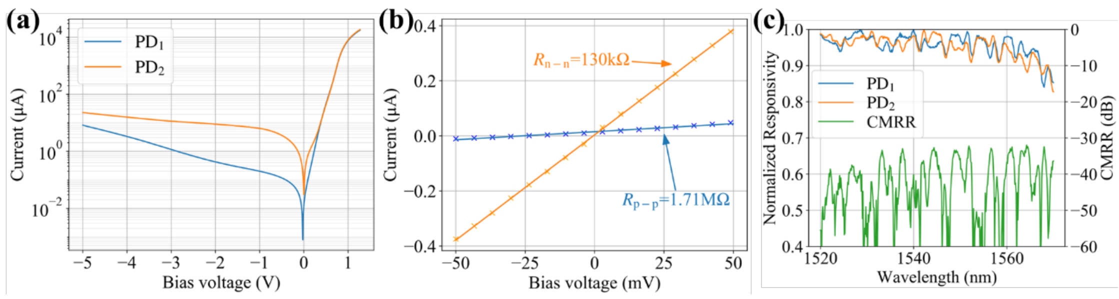

Figure 4 – (a) IV characteristics of individual photodiodes, (b) IV characteristics around 0V in linear scale, and (c) wavelength-dependent responsivity and CMRR values

The normalized wavelength-dependent responsivity of each PD is shown in Figure 4(c). The responsivity of both PDs are stable within ~ 0.5 dB from 1520 nm until 1560 nm, after which the absorption of the active material starts to decrease. Minor oscillations observed in the wavelength response occur are interference patterns due to small reflections in the WGs leading to the PDs. The common-mode rejection ratio (CMRR) is defined as, CMRR = 20log $[(R_{PD1} - R_{PD1})/(R_{PD1} + R_{PD1})]$ where R_{PD1} and R_{PD2} denote the respective responsivity of each photodiode. CMRR of below −30 dB is achieved across the whole measurement range. The photocurrent is around 300 μA for both PDs for a TEpolarized input power set at 10 dBm at 1550 nm. Assuming the PDs have a similar responsivity to the previously reported value of 0.85 A/W [8], and an additional 5 dB loss to the fiber coupling and WG loss; we think the remaining ~ 9 dB loss is due to the optical mismatch at the butt-joint interfaces of the n-n isolation sections, because of the topology formed by local epitaxial growth rate enhancement. This loss has to be reduced to below 1 dB to be acceptable and will require further process development.

Figure 5(a) shows the response of each PD at 1550 nm at 0V bias as a function of the input signal frequency. The resulting CMRR values stay below −25dB for the measurement range. Balanced PDs with similar structure and varying absorption region length are fabricated on the same die to compare their high-speed performance. Figure 5(b) shows the 3-dB bandwidth of PDs with 30, 60 and 100 µm length under applied reverse bias. The bandwidth increases up to 15 GHz for 30 µm-long PDs at −7V.

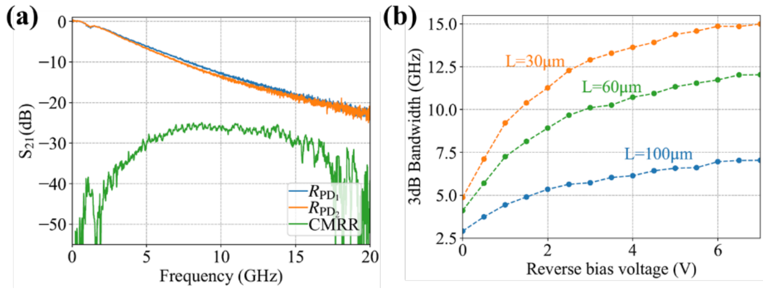

Figure 5-(a) High-speed response of each photodiode at 1550nm under zero bias. (b) 3-dB bandwidth of PDs with varying absorption region length as a function of applied reverse bias

Conclusion

Balanced PDs have been designed and fabricated using an extension over the standard process of SMART Photonics, developed to locally replace the n-InP with SI-InP under the Q1.25 layer, preventing parasitic connections. The fabricated balanced PDs have a flat responsivity over the wavelength range of 1530 nm-1570 nm and their wavelength dependent CMRR is below −30 dB. The measured 3-dB bandwidths are up to 15 GHz and the modulation-frequency dependent CMRR is below −25 dB.

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