Heterogeneous integration of low voltage III-V electro-absorption modulator and driver for optical I/O by micro-transfer printing

H. Li[1,3], B. Pan[1,3], J. Zhang[1,3], T. Pannier[2], L. Bogaert[1,3], P. Ossieur[2], G. Roelkens[1,3]

[1] Photonics Research Group, INTEC, Ghent University - imec, 9052 Ghent, Belgium
[2] IDLab, INTEC, Ghent University - imec, 9052 Ghent, Belgium
[3] Center for Nano- and Biophotonics, Ghent University - imec, Ghent, Belgium

Scaling workloads for multi-GPU systems requires co-packaged CMOS compatible optical I/O. We proposed the design of a compact Electronic-Photonic Integrated Circuit (EPIC) through micro-transfer printing (µTP) of Indium Phosphide (InP) electro-absorption modulators (EAMs) and electronic driver chiplets onto a silicon photonics substrate. The footprint of the transmitter EPIC unit is 500 × 500 µm², including 300 × 200 µm² for the driver and 500 × 100 µm² for the EAM. The modulator operates in O-band with the multi-quantum wells (MQWs) active region on InP. Light is coupled evanescently from the silicon waveguide to the InP modulator using a taper structure optimized by particle swarm optimization, achieving a coupling efficiency of over 90%, even with a misalignment of up to 0.5 µm. The MQWs are designed to be compatible with CMOS driving voltages (1 V bias and 0.8 V swing). Additionally, the device is engineered to function at 32 Gbps Non-Return-to-Zero (NRZ), delivering an optical modulation amplitude (OMA) greater than 0.32 mW for 1mW optical input power.

Introduction

With the rapid expansion of artificial intelligence, high-performance computing, data centers, and telecommunications, there is an urgent need for innovative solutions to meet the increasing demands for high bandwidth, low latency, and low power consumption. Integrating photonics closer to compute units through co-packaged optics and optical I/O offers a promising approach to overcome the limitations of traditional electrical connections.

µTP is an advanced heterogeneous integration technique that enables the addition of diverse functionalities to a target platform using polydimethylsiloxane (PDMS) polymer stamps, effectively addressing the platform's functional limitations. In this work, we propose a design for an O-band InP-based MQW EAM utilizing µTP. With careful optimization, the modulator operates at low voltages, making it compatible with CMOS technology, and can deliver NRZ signals at 32 Gbps. Additionally, it is also possible to place printable electronics [1] adjacent to the EAM to further minimize connection parasitic, incorporating terminated resistors on silicon photonics.

Design and simulation

In the beginning, we need to define the EAM layer stack. To achieve low power consumption, both the bias voltages and swing have to be reduced. Based on the absorption profile of an InP EAM multi-quantum well stack, to achieve a higher OMA we aim to shift the electric field sweep range to the right side of the curve in Fig.1 without reaching the breakdown electric field. This adjustment requires reducing the thickness of the intrinsic layer accordingly.

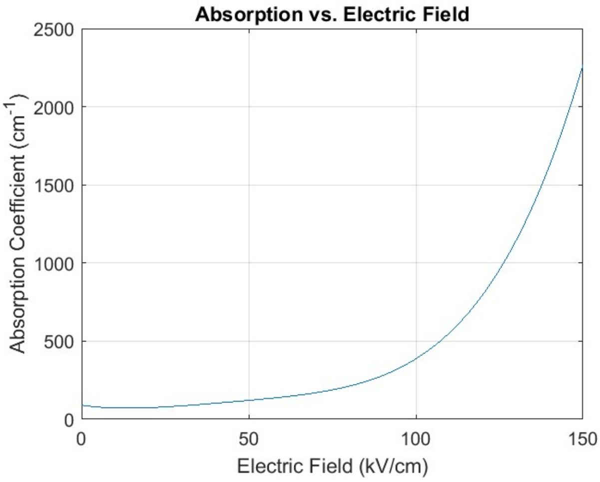

Fig. 1: Absorption coefficient versus electric field intensity.

The separate confinement heterostructure (SCH) layer is therefore set at 30nm to improve the RF performance and achieve good confinement (Fig. 2). Reducing the number of layers could also help, but the interaction of light with the MQW stack will also drop. Another solution is to keep MQW numbers unchanged but add partial doping in the SCH layer. To reduce the loss from p-InGaAs and p-metal but maintain relatively low series resistance, the thickness of the p-cladding is chosen to be 1.5 μm.

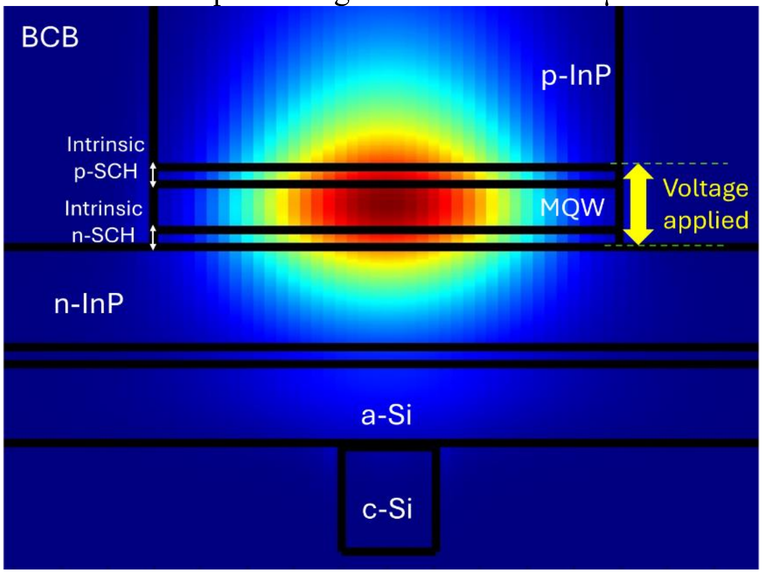

Fig. 2: Cross sections of active region and mode profile

In the optimization process, bandwidth (BW) requirements must also be considered. For a given width and length of the active rib waveguide planarized by BCB, the bandwidth is proportional to the thickness of the intrinsic layer. Balancing these competing parameters, we set boundary conditions with an electric field limit of 150 kV/cm and a minimum bandwidth requirement of 25 GHz. Any OMA optimization exceeding these boundaries is disregarded (set to zero in optimization).

The photonic structures beneath the μTP EAM also contribute to OMA, by manipulating the mode profile and reducing the loss from the p-metal, although it also slightly lowers confinement in the MQWs. The target platform influences both coupling and active performance, so we include the geometries of both the III-V and silicon photonic structures in the active region to optimize for OMA. The bias sweep is conducted within a range over half the voltage swing to avoid forward bias voltages.

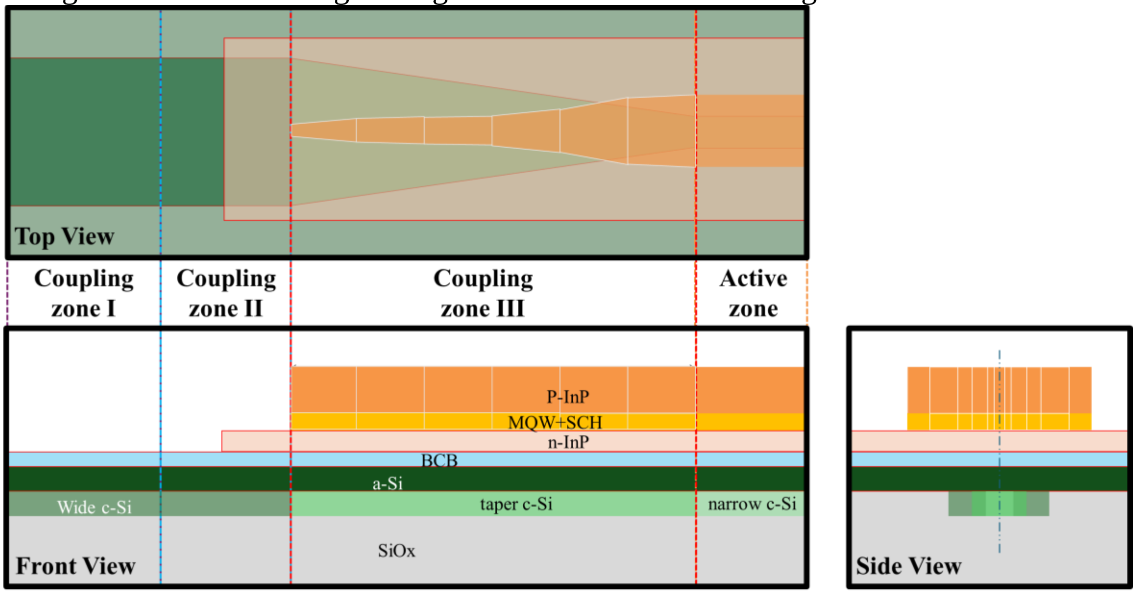

Fig. 3: Coupling taper structures

For the µTP EAM, light travels from the waveguide to the III-V layer and then back to the waveguide after modulation, introducing two instances of coupling loss. Consequently, a robust coupling scheme is essential for effective heterogeneous integration. A directional coupler could be compact, but it lacks robustness against misalignment. Here, we introduce a taper coupler to improve the coupling between the III-V and silicon (Fig. 3). Particle swarm optimization was applied on the taper design to achieve an intrinsic taper coupler loss of 0.66 dB per pass. This configuration yields an OMA of 0.32 mW with an input power of 1 mW. Fig. 4 shows how an active length of 84 µm provides the largest OMA, while a length of 99 µm maximizes ER, both meeting the 25 GHz BW requirement required for 32 GBd NRZ.

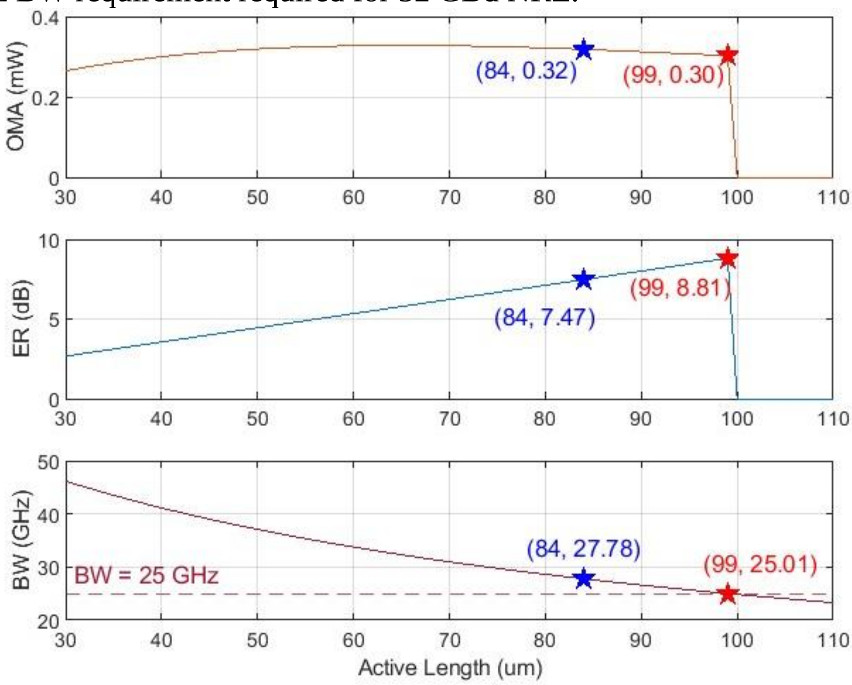

Fig. 4: Trend of OMA, ER, BW in relation to active length.

Driver integration

Heterogeneous integration of electronics and photonics through μTP, as demonstrated in [1], offers the possibility of closely integrating a driver amplifier with the EAM. These electronic chiplets can be put underneath a GPU and connected via solder bumps to the GPU to realize optical I/O [2]. The thickness of the chiplets is around 20 μm in height, we can therefore connect the driver to the EAM with short metal traces, further reducing resistance and capacitance (Fig. 5).

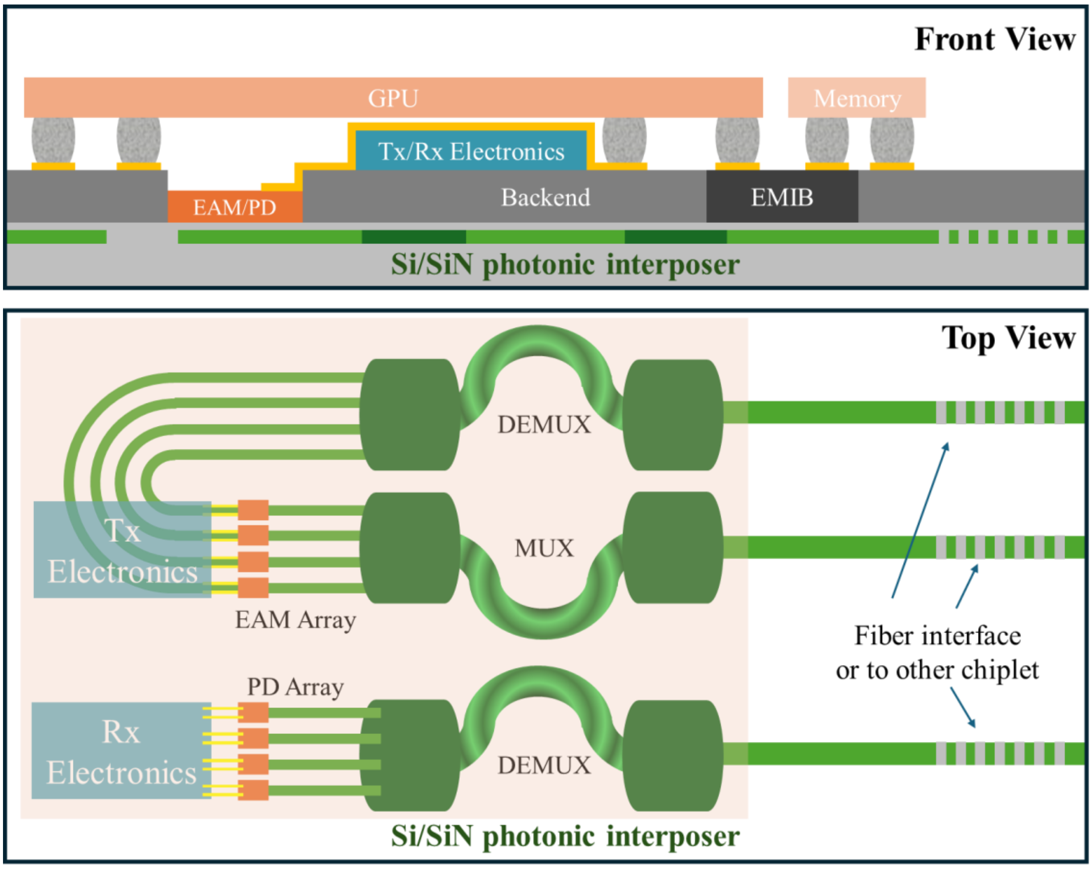

Fig. 5: Optical IO for GPU interconnect [2]

Conclusion and future work

In this paper, we propose a design for a low drive voltage EAM heterogeneously integrated on a silicon photonics platform. Through optimization of the III-V epitaxial layers, the active region geometry and the taper design, simulations indicate an OMA of over 0.32 mW (1 mW input) at a bias of 1 V and a swing of 0.8 V can be achieved. By employing μTP, we can integrate electronics adjacent to the photonic circuit, paving the way for advanced electronic-photonic integrated circuits for optical I/O.

References

[1] R. Loi *et al.*, "Micro transfer printing of electronic integrated circuits on Silicon photonics substrates," 2022.

[2] S. Zhang *et al.*, "Photonic Network-on-Wafer for Multichiplet GPUs," *IEEE Micro*, vol. 43, no. 2, pp. 86–95, Mar. 2023