Towards monolithic multilayer integration in the Al_2O_3 platform

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In this work, we propose the monolithic integration process of active-passive devices in the Al_2O_3 platform. As proof of concept, we aim to integrate an Al_2O_3 passive WDM device with an active Al_2O_3: Er^{3+} spiral waveguide amplifier. Simulations using Lumerical will be carried out to optimize the dimensions of the waveguides and the tapers to obtain an adiabatic transition of the fundamental TE mode. The proposed fabrication process involves: RF reactive sputter deposition of Al_2O_3 and Al_2O_3:Er^{3+} layers, (EBL) lithography, and RIE etching to pattern the waveguides. In addition, a CMP process is optimized to level the LPCVD layer. Lastly a PECVD layer is deposited to clad the structure. The gain and noise figure for a 1550 nm signal with bidirectional pumping at 1480 nm will be reported.

1. Introduction

Targeting more than Moore's low, photonic integrated circuits (PICs) are following the path of electronics by inserting new materials as the Al_2O_3 platform to the nanotechnology fabrication process and by integrating many functions on the same chip as amplifiers, modulators and filters using passive and active devices as well.

Monolithic integration is an effective method to integrate different active and passive functionalities on the same PIC resulting in compact devices and high throughput while reducing the production cost and the complexity of assembly methods.

Over the last decade several active-passive devices have been developed. A high gain (>25 dB) in Al_2O_3:Er^{3+} amplifiers integrated with silicon nitride circuits in a multi-layer platform was demonstrated [1].An optical amplifier in Al_2O_3: Er^{3+} monolithically integrated on the Si_3N_4 platform was demonstrated with a net gain of 18.1±0.9 dB at 1532 nm, and a broadband gain operation over 70 nm covering wavelengths in the S-, C- and L-bands [2]. In this work we present our optimization results of the CMP step which is essential to the monolithic integration.

2. Methodology

2.1 proposed fabrication process

The proposed fabrication process, shown in figure (1), starts by depositing a passive Al_2O_3on a thermal SiO_2 substrate using RF reactive sputter deposition, followed by an electron beam (EBL) lithography step and RIE etching process to microstructure the passive components. Subsequently, a SiO_2 spacer layer is deposited using LPCVD, followed by a CMP process to planarize the surface making it ready to deposit the erbium doped Al_2O_3 layer again by RF reactive co-sputtering. After patterning the waveguide spiral amplifier using EBL lithography and RIE etching, a layer of SiO_2 (LPCVD+PECVD) is deposited to clad the structures. Lastly, thermal annealing is applied to improve the performance of the device.

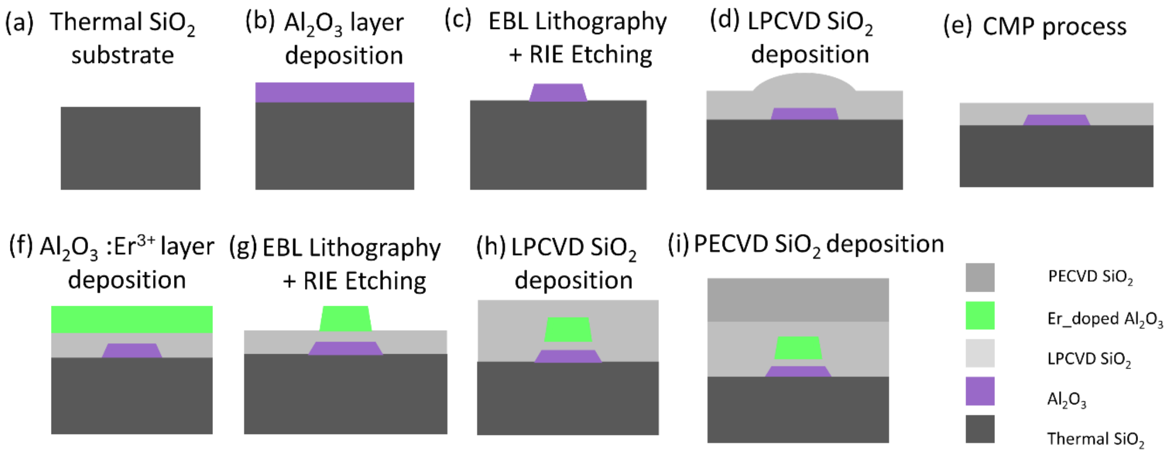
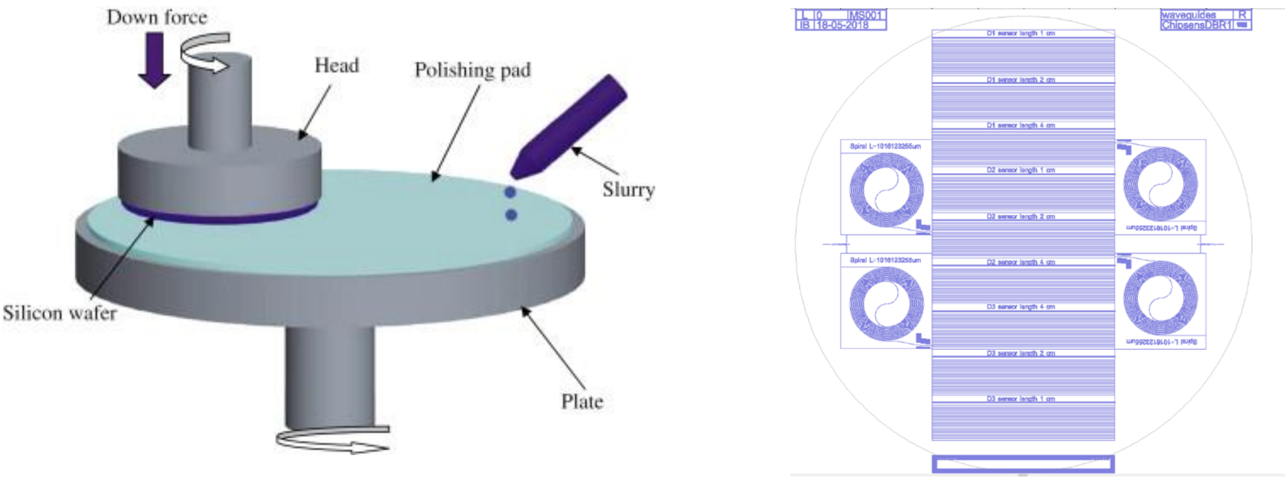


Figure (1): The proposed fabrication process.

2.2 CMP optimization

Figure (2.a) illustrates the Chemical Mechanical Polishing (CMP) process used to level the LPCVD layer deposited on top of the Al_2O_3 waveguides. CMP plays a crucial rule when coming to the surface roughness of the LPCVD layer which influences the deposition of Al_2O_3: Er^{3+} layer on top. Figure (2.b) as well, shows the mask layout used to pattern the test structures which consist of ~ 1 µm thick SiO_2 waveguides covered by ~2 µm SiO_2 cladding on top of a silicon wafer.



(a) (b)

Figure (2): a. Schematic of the CMP process, the image is taken from [3]. b. The mask layout of the structure.

To obtain a high polishing rate and a good surface quality, we used the values shown in table (1) then we investigated the effect of the following mechanical process parameters: (1) the work pressure of the CMP machine, (2) the rotation speed of both the pad (plate) and the head, and (3) the duration of the polishing process. These parameters are shown in table (2).

Back Pressure [bar]	Work Pressure 1 [bar]	Work Pressure 3 [bar]	Work Pressure 4 [bar]	Timer 1 [s]	Timer 3 [s]	Timer 4 [s]
0,2	0,4	0,5	0,41	5	1	60

Table (1): Values of the constant parameters used during the CMP process.

Wafer ID	Work Pressure 2 [bar]	Timer 2 [s]	Rotation Speed [rpm]	Surface Removed Thickness Range [nm]	Structure Removed Thickness Range [nm]
Si1145 (CMP1)	0,6	60	Pad speed=55 Head speed=55	50-90	Wafer's Center: 600-950 Wafer's Edge: 600-925
Si1145 (CMP2)	0,6	60	Pad speed=55 Head speed=55	40-90	Wafer's Center: 300-75 Wafer's Edge: 275-65
Si1136	0,7	60	Pad speed=55 Head speed=55	45-130	Wafer's Center: 600-990 Wafer's Edge: 600-950
Si1106	0,79	90	Pad speed=85 Head speed=78	130-190	Wafer's Center: 925-1000 Wafer's Edge: 925-1000
Si1130	0,8	60	Pad speed=55 Head speed=55	70-135	Wafer's Center: 725-990 Wafer's Edge: 800-985
Si1260	0,9	60	Pad speed=55 Head speed=55	65-145	Wafer's Center: 650-925 Wafer's Edge: 750-975
Si1261	1,0	60	Pad speed=55 Head speed=55	110-220	Wafer's Center: 850-995 Wafer's Edge: 900-995
Si1123	1,0	40	Pad speed=55 Head speed=55	40-115	Wafer's Center: 500-950 Wafer's Edge: 500-950

Table (2): Values of the parameters changed for the CMP process optimization.

A silica-based slurry is used for the CMP process. After polishing, an RCA-1 cleaning process is applied on the wafers. To measure the thickness of the LPCVD surrounding layer, an ellipsometer (Woollam M-2000UI) is used before and after polishing as shown in figure (3). Also, the step height of the structures is measured using a profilometer (Veeco Dektak 8) and shown in figure (4). Lastly, images using AFM are taken as in figure (5) which shows that the surface roughness has improved from 2.52 nm to 0.453 nm.

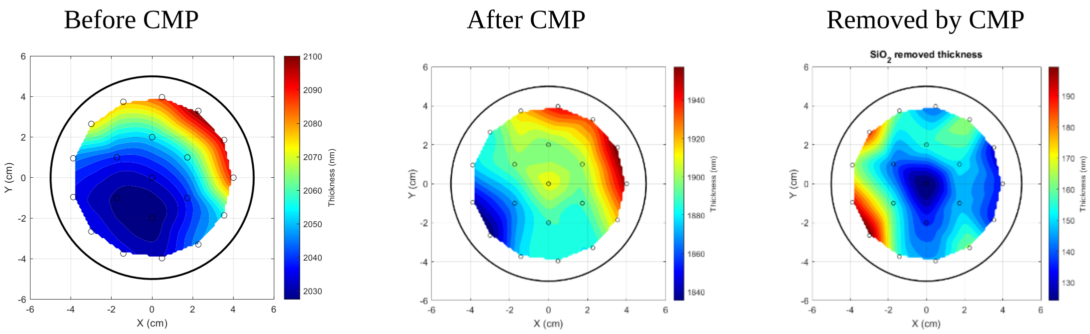


Figure (3): The surface thickness of the SiO_2 layer.

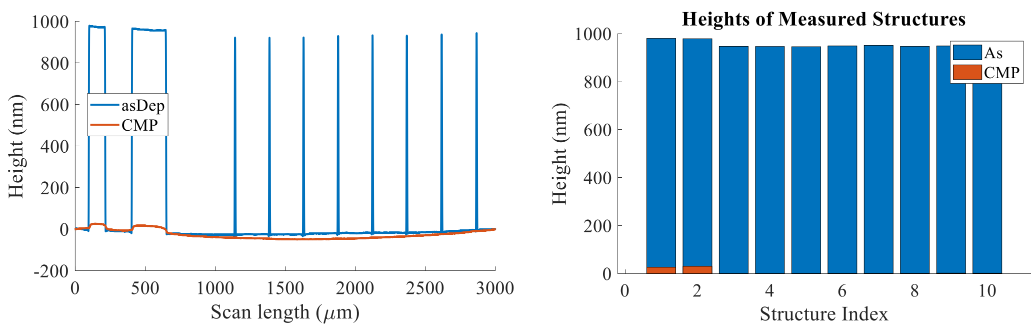


Figure (4): The step height of the structures in the SiO_2 layer.

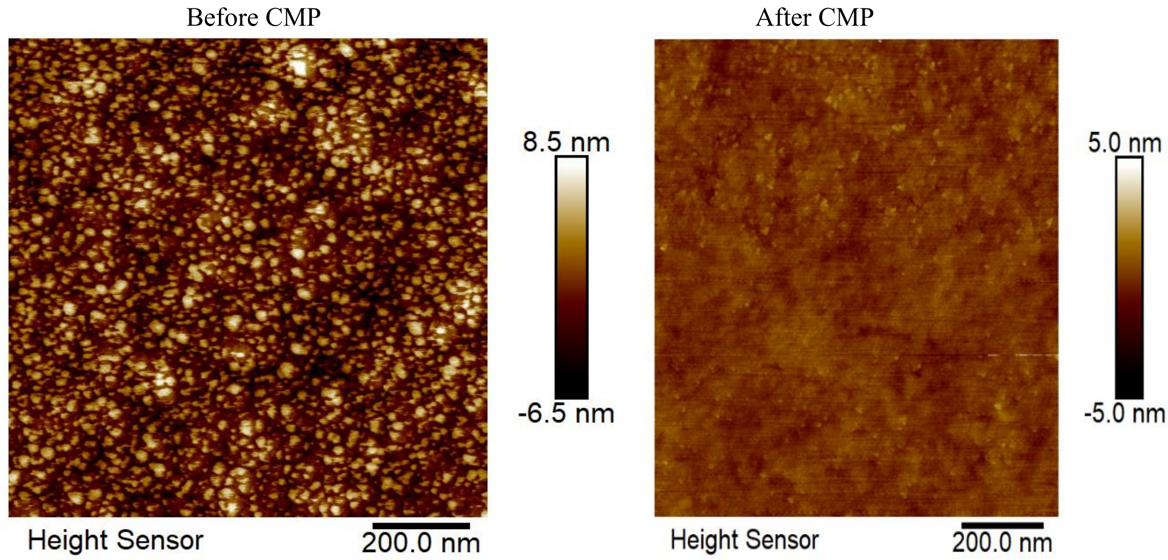


Figure (5): The surface roughness of the LPCVD SiO_2 layer.

The results shown in figures (3), (4) and (5) belongs to the best case where the pad speed rotation is 85 rpm, the head speed rotation is 78 rpm, work pressure is 0.79 bar, and the duration of the process is 90 s.

3. Further work

Simulations using Lumerical will be carried out to optimize (1) the dimensions of the waveguides in both layers Al_2O_3 and Al_2O_3: Er^{3+}; (2) the thickness of the oxide layer spacer between the two layers; (3) the dimensions of the two vertical tapers, which are designed to obtain an adiabatic transition of the fundamental TE mode; (4) the WDM for 1480/1550 nm wavelength.
The gain and noise figure for a 1550 nm signal with bidirectional pumping at 1480 nm will be reported.

4. Conclusion:

In this work, CMP process was optimized to level the LPCVD cladding where the pad speed rotation was 85 rpm, the head speed rotation was 78 rpm, work pressure was 0.79 bar, and the duration of the process was 90 s.

By developing the process of integrating multilayers in the Al_2O_3 platform, many other devices and functions in many fields like communication networks [4], light detection and ranging (LIDAR) applications [5] and biological sensing [6] can be fabricated benefiting from the properties of Al_2O_3 such as the very broad transparency window which spreads from UV to mid IR, the low propagation losses, and the high solubility of rare-earth ions which give high optical gain in different spectral ranges.[7]

References:

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